DEVICE ENGINEERING OF ORGANIC FIELD-EFFECT TRANSISTORS

TOWARD COMPLEMENTARY CIRCUITS

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DEVICE ENGINEERING OF ORGANIC FIELD-EFFECT TRANSISTORS

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SUMMARY

Organic complementary circuits are attracting significant attention due to their high power efficiency and operation robustness, driven by the demands for low-cost, large-area and flexible devices. Previous demonstrations of organic complementary circuits often show high operating voltage, small noise margins, low dc gain, and electrical instability such as hysteresis and threshold voltage shifts. There are two obstacles to developing organic complementary circuits: the lack of high-performance *n*-channel OFET devices, and the processing difficulty of integrating both *n*- and *p*-channel organic field-effect transistors (OFETs) on the same substrate. The operating characteristics of OFETs are often governed by the boundary conditions imposed by the device architecture, such as interfaces and contacts instead of the properties of the semiconductor material. Therefore, the performance of OFETs is often limited if either of the essential interfaces or contacts next to the semiconductor and the channel are not optimized.

This dissertation presents research work performed on OFETs and OFET-based complementary inverters in an attempt to address some of these knowledge issues. The objective is to develop high-performance OFETs, with a focus on *n*-channel OFETs through interface engineering both at the interface between the organic semiconductor and the source/drain electrodes, and at the interface between the organic semiconductor and gate dielectric. Through interface engineering, both *p*- and *n*-channel high-performance low-voltage OFETs are realized with high mobilities, low threshold voltages, low subthreshold slopes, and high on/off current ratios. Optimization at the gate

dielectric/semiconductor also gives OFET devices excellent reproducibility and good electrical stability under multiple test cycles and continuous electrical stress. Finally, with the interfaces and contacts optimized for both *p*- and *n*-channel charge transport, the integration of *n*- and *p*-channel OFETs with comparable performance are demonstrated in complementary inverters. The research achieves inverters with a high-gain, a low operation voltage, good electrical stability (absence of hysteresis), and a high switching-speed. A preliminary study of the encapsulation of OFETs and inverters with an additional protective layer is also presented to validate the practicality of organic devices containing air-sensitive *n*-channel transport.

CHAPTER 1 INTRODUCTION

Chapter 1 introduces organic semiconductors, organic field-effect transistors (OFETs), and complementary inverters based on OFETs. The progress in the development of OFETs and OFET-based inverters is reviewed, and the challenges and the current issues during the development are listed. The motivation for the current research is also described, and particular issues of interest related to the current research are identified. The objectives and the organization of the research dissertation are also included.

1.1 Organic Semiconductors and Organic Field-Effect Transistors

1.1.1 Organic Semiconductors

Semiconductors based on organic molecular components are mainly composed of hydrogen, carbon, and oxygen. Unlike inorganic semiconductors that are crystalline with band-like charge transport, organic semiconductors are amorphous or polycrystalline in which the charge transport occurs through hopping of charges between delocalized π molecular orbitals.

The semiconducting or conducting properties of organic moelcules can be attributed to the special chemical characteristic of carbon: carbon atoms can form double bonds between each other, as shown in Figure 1.1. One is known as a σ bond formed by the overlap of hybridized sp^2 orbitals, and the second is know as a π bond formed by the overlap of the remaining unhybridized p_z orbitals. The σ electrons always remain between the carbon atoms, while the π electrons are delocalized over the neighboring

molecules in a conjugated system, by which the electrons can gain some freedom to move along the entire chain. The formation of delocalized π molecular orbitals defines the frontier electronic levels: the highest occupied molecular orbital (HOMO) and the lowest unoccupied molecular orbital (LUMO). The HOMO and LUMO levels determine the electrical and optical properties of the organic semiconductor molecules.

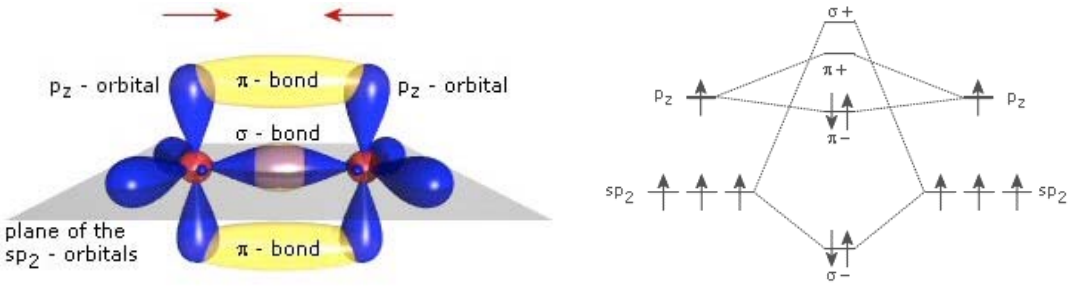


Figure 1.1: Scheme of the orbitals and bonds for two sp_2 hybridized carbon atoms [1].

Based on different basic units, organic semiconductors can be categorized into two groups: small-molecule organic semiconductors and polymer organic semiconductors. In small-molecule organic semiconductors, the carbon atoms form larger molecules typically with benzene rings as the basic unit and π electrons become delocalized through the molecules, as shown in Figure 1.2(a). The molecular weight of small-molecule semiconductors is usually less than 1000 g/mol. In polymer organic semiconductors as in Figure 1.2(b), the carbon atoms form a long chain and π electrons become delocalized along the chain and form a one-dimensional π-conjugated system. The molecular weight of polymeric semiconductors is usually greater than 1000 g/mol.

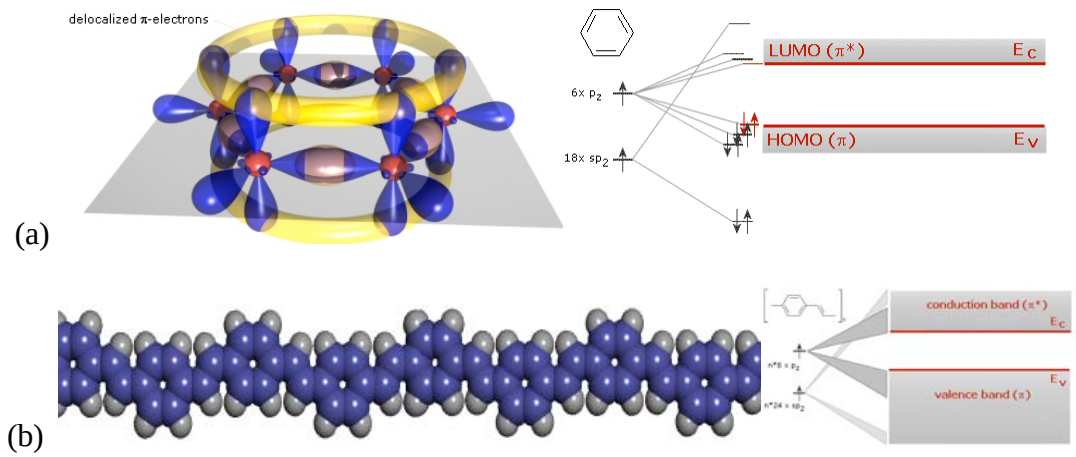


Figure 1.2: (a) Scheme of a benzene ring and energy structure of small-molecule organics. (b) Scheme of a polymer subunit and the energy structure of polymer organics [1].

The discovery of electrical conduction in organic solids dates back nearly 100 years with the observation of photoconductivity and the study of the dark conductivity in anthracene crystals [2, 3]. In 1977, the first highly conducting polymer, chemically and electrochemically doped polyacetylene, was discovered by Heeger, Shirakawa, and MacDiarmid, which won them a Nobel Prize in Chemistry in 2000 [4]. This remarkable observation opened up an entire new field called organic electronics, and a new range of applications for conducting and semiconducting organic materials. Organic electronics generally refers to electronic devices and systems that are based on organic semiconductors, and generally it is applied to three main technological areas: organic light-emitting devices (OLEDs), organic photovoltaic solar cells (referred as OSCs or OPVs), and organic electronic circuits based on organic thin-film field-effect transistors (referred as OTFTs or OFETs). In May 2008, Sony unveiled an ultra-thin 11 inch OLED TV with high energy efficiency and brightness [5]. OLEDs could compete with and

eventually replace white and blue GaN-based light-emitting diodes (LEDs) used in mobile phone displays since they do not require backlighting. OPVs are envisioned as future power supplies for large-scale power generation [6]. OFETs have recently gained attention as building blocks for electronic applications that can greatly benefit from low-cost, large-area fabrication and flexible form factors, such as radio-frequency identification tags (RFID) [7], drivers for electronic paper [8] and driving circuits for flat panel displays (FPDs) [9].

1.1.2 OFETs vs. Inorganic Thin-Film Transistors

OFETs, thin-film transistors (TFTs) with organic semiconductors as the active layers, are of great interest as a potential alternative to amorphous Si (α-Si) TFTs. With remarkable progress in the synthesis and purification of organic semiconductors and the processing of these materials into devices, the mobility of the best OFETs has surpassed that of α-Si TFTs [10].

A major advantage of OFETs vs. α-Si TFTs is their compatibility with low-cost, low-temperature processes. A typical α-Si: H TFT fabrication process involves the deposition of hydrogenated α-Si as an active layer and silicon nitride as a gate dielectric by plasma enhanced chemical vapor deposition (PECVD) using H_2/SiH_4 (silane) and NH_3/SiH_4, respectively. The process temperature is usually much higher than 250 °C, which enables the use of inexpensive glass as substrate [11]. However, this fabrication process is not compatible with colorless, transparent flexible polymeric substrate materials, which typically require a temperature below 200 ºC. OFETs, on other hand, can be processed at much lower temperatures using various simple, low cost techniques, including vacuum thermal evaporation, spin-coating, dip-coating, vapor deposition,

microcontact printing, screen-printing, etc. The combination of low-temperature processibility with the mechanical flexibility of organic materials thus leads to a wide range of applications in flexible electronics with a potential for very low cost manufacturing.

Secondly, α-Si technology provides only high performance *n*-channel transport which prevents the use of complementary metal–oxide–semiconductor (CMOS) technologies. In contrast, the versatility of synthetic organic chemistry has enabled the tailoring and engineering of both *n*- and *p*-type semiconductors, giving rise to many potential candidates for circuit designs based on CMOS technology.

1.2 Review of Progress in OFETs and OFET-Based Complementary Inverters

1.2.1 Progress in OFETs

Pioneering work on OFETs started in 1983 by Ebisawa using polyacetylene as an active semiconductor [12]. A few years later in 1986, Tsumura demonstrated an OFET with polythiophene in which a large modulated current was obtained [13]. Then, OFETs using poly (3-hexylthiophene) as an active semiconductor were reported in 1988 [14]. Most of these early OFETs were fabricated using thin films of polymeric semiconductors formed from solution by spin coating, screen printing or inject printing. The polymer films are typically amorphous, and the carrier mobility is rather low, ranging from 10^{-5} to 10^{-4} cm^2/Vs. In contrast, small-molecule semiconductors can be deposited from a gas phase by vacuum thermal evaporation or by organic vapor phase deposition and the molecules can pack into well-organized polycrystalline films, which leads to higher

carrier mobility. Another advantage of small molecules is that their charge transport can be controlled by modifying various molecular parameters and deposition conditions.

In 1989, Horowitz *et al*. demonstrated the first OFET using a small-molecule semiconductor α-sexithiophene [15] with a higher carrier mobility of 10^{-3} cm^2/Vs and an on/off current ratio of 10^5. Pentacene, the most important small-molecule semiconductor so far, was applied to OFETs in 1991 [16, 17]. By 1997, pentacene OFETs had achieved a high carrier mobility of 1.5 cm^2/Vs and an on/off current ratio of 10^8, which are comparable with the electronic performance of hydrogenated α-Si TFTs [18]. Later on in 2003, 3M reported pentacene OFETs with a field-effect mobility value up to 7 cm^2/Vs [19]. However, most groups can only routinely obtain mobility around 1cm^2/Vs with thin-film pentacene.

All the semiconductors mentioned above are *p*-type in which the conduction in the materials is due to the positively charged carriers. However, in order to realize applications such as organic complementary logic circuits [20], both *p*-type and *n*-type organic semiconductors are needed with comparable electrical performance. A small number of *n*-type organic materials in which the conduction is due to the negatively charged carriers have been investigated, including fullerene C_{60} (buckminsterfullerene or buck balls) [21-27], fluorocarbon-substituted thiophene oligomers [28-30], naphthalene and perylene derivatives [31-33], etc. Among these *n*-type organic semiconductors, C_{60} holds promise for high-mobility *n*-type OFETs since Haddon [21] first reported it in 1995. Electron mobilities as high as 4.9 cm^2/Vs and 6 cm^2/Vs have been reported by Itaka [26] and Anthopoulos [25], both using C_{60} as active materials. However, the on/off current ratio in the former was inevitably reduced with pentacene (a well-known *p*-type

semiconductor) at the dielectric/semiconductor interface. In the latter report, C_{60} was deposited by hot wall epitaxy (HWE) requiring undesirably high deposition temperatures up to 250 ºC. On the other hand, the issue with high threshold voltage in *n*-type OFETs, which greatly hinders its application in circuit operation, has not been addressed in both cases.

1.2.2 Progress in Organic Complementary Inverters

To realize practical organic electronic devices, a complementary device architecture (utilizing both positive and negative gate bias to turn transistors on and off) is of great interest. The very first results on complementary organic circuits were reported by Dodabalapur in 1996 [34] and Lin in 1999 [35], both from the Bell Laboratories. A short time later, Crone [36, 37] demonstrated the design and fabrication of large-scale complementary integrated circuits based on organic transistors. The static power dissipation was greatly reduced compared to the *p*-channel only technology. With similar methods, more organic complementary inverters based on different materials [33, 38-41] have been reported with a relatively high gain (>10) and an output voltage swing close to the supply voltage, demonstrating the enhanced circuit stability of complementary circuits compared to *p*-channel logic. However, the required supply voltage (V_{DD}) for these inverters was relatively high ($|V_{DD}| > 40$) for practical applications, mostly due to the high threshold voltage and low mobility of *n*-channel OFETs.

Low-voltage organic complimentary circuits have also been developed using thin gate dielectrics [42, 43], a double-gate structure (top-gate and bottom-gate) [44], and patterned *n*- and *p*-type semiconductors by means of integrated shadow masks [45]. Among these methods, increasing the capacitance density of the gate insulators using thin

gate dielectrics can effectively lower the operating voltage [42, 43]. In particular, Klauk [43] demonstrated ultra-low power consumption complementary circuits operating between 1.5 and 3.0 V using ultra-thin Al_2O_3 treated with a self-assembled monolayer (SAM) as gate dielectrics. However, as in previous reports of organic complementary circuits [42, 45], F_{16}CuPC *n*-channel OFETs often show inferior performance compared to their counterparts (pentacene *p*-channel OFETs) with a mobility more than one order of magnitude lower. Complementary inverters with comparable mobilities and threshold voltages were reported using pentacene *p*-channel OFETs and C_{60} *n*-channel OFETs. With matched performance in both transistors, the switching voltage of the inverter can be as low as 1.5 V with a dc gain as high as 150 [46]. However, the inverter showed a large hysteresis in the transfer characteristics indicating high trapping density at the dielectrics, which induces electrical instability upon operation.

Complementary-like organic circuits have also been demonstrated with ambipolar OFETs that are capable of operating in either the *n*- or *p*-channel region. Various structures were proposed and employed in the realization of ambipolar OFETs, including an interpenetrating network structure with a blend of *n*- and *p*-type semiconductors [47-49], a heterostructure of *n*- and *p*-type small-molecule organic semiconductors [50-53], and pure semiconductors with a narrow band gap [30, 54-56]. Although some ambipolar inverters do behave complementary-like with some level of small-signal gain [47, 56, 57] (>10), this technology is not truly complementary. The biggest problem is that the inverter cannot be completely switched on and off, which in turn leads to undesirable static power consumption. In addition, with only one semiconductor, it is almost

impossible to match parameters such as field-effect mobility and threshold voltage (V_T) for both the *n*- and the *p*-channel OFETs.

1.3 Current Issues in the Development of Organic Complementary Inverters

The major advantages of complementary circuits over *n*- or *p*-channel only circuits and systems include [58-60]:

- Lower power dissipation, especially static dissipation in digital systems,
- Signal voltages that can easily swing from one power supply voltage to the other,
- A system with increased tolerance of variations in transistor parameters,
- Higher circuit gain, leading to larger noise margins in digital systems, and
- Simpler and easier design methods.

To take full advantage of CMOS technology, organic complementary circuits require both *n*- and *p*-channel OFETs with comparable performance, including mobilities, threshold voltages, subthreshold slopes (also called subthreshold swing), and on/off current ratios. These requirements are critical since the system performance will be otherwise limited to that of the transistors with inferior performance. Therefore, a low-mobility *n*-channel OFET in a CMOS inverter must be scaled to a larger width to provide channel current comparable with that of the *p*-channel OFETs. Consequently, the operating frequency will be decreased since the large *n*-channel devices dominate the gate input capacitances.

Despite the fact that power efficiency and robustness are becoming more important in organic electronics, the majority of the organic circuits reported to date use *p*-channel

transistors only. There are two obstacles in developing organic complementary circuits: the lack of high-performance *n*-channel OFET devices and the process difficulty of integrating both *n*- and *p*-channel OFETs on the same substrate.

In order to exhibit good electrical performance, OFETs should display high drain current at low drain and gate voltages (without reliance on optimized geometric factors), high on/off current ratios (which requires that drain current at V_{GS} = 0 should be extremely low), and fast switching speed. Despite significant improvements in the electrical characteristics of OFETs, the majority of *n*-channel OFETs showed inadequate electrical performance, such as low mobility, high threshold voltage, and high operating voltage.

It has been acknowledged that carrier mobility correlates with the purity of the organic semiconductors in which the impurities or unintentional dopants needed to be removed by extensive purification processes. However, in most cases, the operating characteristics of OFETs are governed not only by the properties of the semiconductor material but also by the boundary conditions imposed by the device architecture, such as interfaces and contacts. The performance of OFETs is often limited if either of the essential interfaces or contacts next to the semiconductor and the channel is not optimized.

The interface at the gate dielectric/semiconductor has profound influence on the morphological formation of the semiconductor film and the charge transport along the channel [61, 62]. In the case of *n*-channel OFETs, electron trapping at the interface by carbonyl, hydroxyl, and silanol groups has been confirmed as a primary limiting factor for *n*-channel conduction and a major contribution to large threshold voltage [63, 64].

SAMs as surface modification materials for dielectric surfaces can induce beneficial change in the film morphology of the active semiconducting layer, and at some level can provide a barrier for the trapping effect and other adverse sites at the interface. However, SAMs cannot form a full coverage over the surface and passivate the adverse effect. The formation of uniform, orderly, and high coverage SAM layers has posed many challenges in film processing.

Parasitic and non-linear effects, which often occur at the contact between the semiconductor and the gate dielectric, have been reported as an important factor causing the limited electrical characteristics in OFET operation. The microscopic origin of these effects are not widely understood, which may be a general representation of the effects present in OFETs operations, including a non-ohmic contact between metal contacts and organic semiconductors, higher charge carrier traps at the interfaces, disturbed film growth at the interfaces, and so on. Some are introduced during materials processing or result from the device design. Others are intrinsic to specific materials used in OFET fabrication or otherwise. Among them, high contact resistance causes very low electron mobility in *n*-channel OFETs. Imposed by the injection barrier height between the *n*-type organic semiconductors and the source and drain electrodes, this high contact resistance can greatly limit the switching frequency of the *n*-channel OFETs due to a significant degradation of effective electron mobility upon channel scaling.

The other reasons for the slow development of *n*-channel OFETs can be attributed to the sensitivity of *n*-type semiconductors to environmental conditions, especially oxygen and moisture. The low work-function metals, which are preferred for electron

injection in *n*-channel transistors, are also very reactive and almost oxidize instantly in ambient condition.

Even though great efforts have been given to develop air-stable *n*-type organic semiconductors with higher LUMO levels that can be aligned with metals with higher work function, the highest mobility reported with improved air stability is still far behind that of the *p*-channel OFETs [33]. An encapsulation layer is required for organic electronics, especially for *n*-channel transporters and active metals, to block water and oxygen molecules from penetrating into the semiconductor and electrode. Although some progress has been reported regarding the encapsulation of OLEDs [65-67] and OPVs [68], very few reports on the encapsulation of OFETs have been made and the majority of them dealt with *p*-channel transistors [69-71]. The only report on the encapsulation of *n*-channel OFETs was demonstrated using an Al_2O_3 insulating layer deposited by radio frequency (RF) sputtering [72], which could potentially cause some initial damage to the organic devices.

After the challenges in developing discrete transistors are identified, the issue regarding the integration of *n*- and *p*-channel OFETs reduces to the optimization of interfaces and contacts for both *n*- and *p*-channel transport. Due to the distinctive difference in the HOMO and LUMO levels of organic semiconductors, a metal with a high work function is favored for hole injection into HOMO levels while a metal with a low function work is favored for electron injection into LUMO levels. However, a common dielectric surface is preferred in order to avoid any change to the delicate dielectric surface during additional patterning processes.

1.4 Objectives and Organization of the Dissertation

The primary objective is to develop high-performance OFETs, with a focus on *n*-channel OFETs, through interface engineering both at the interface between the organic semiconductor and the source/drain electrodes, and at the interface between the organic semiconductor and the gate dielectric, as summarized in Figure 1.3. The current research employs a widely used, commercially available, electron-transporting semiconductor, C_{60}, and a hole-transporting semiconductor, pentacene, as *n*- and *p*-channel active materials, respectively. To identify and realize suitable gate dielectric insulators and source/drain (S/D) electrodes for both *n*- and *p*-channel OFETs, the following three aspects are investigated: first, the correlation among device performance, film morphology and dielectric surface properties (i.e., surface roughness, surface energy, and interface trapping density); secondly, the operational stability under dc stress with different types of dielectric surfaces; third, the contact resistance and energy level alignment between S/D electrodes and the organic semiconductor.

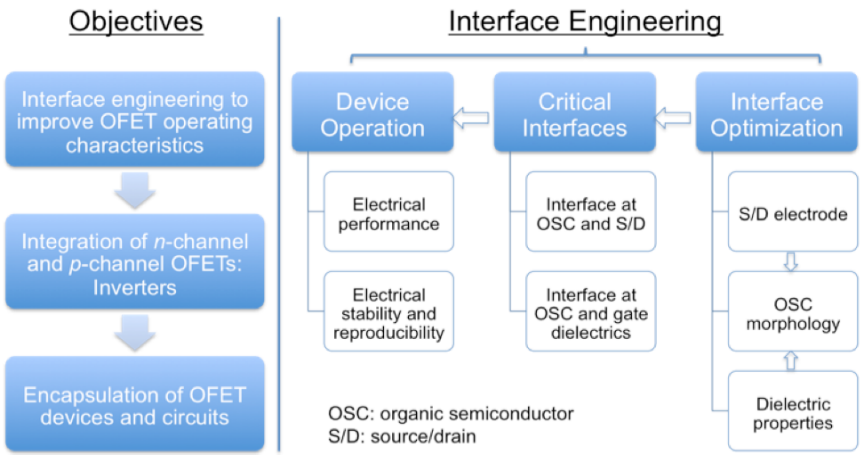


Figure 1.3: Objectives and structure of the current research.

Through device engineering, both *p*- and *n*-channel high-performance OFETs are realized with a high mobility, a low threshold voltage, a low subthreshold slope, and a high on/off current ratio. With an optimized interface at the gate dielectric/semiconductor, the devices also show excellent reproducibility and good electrical stability under multiple test cycles and continuous electrical stress. The contact resistance of these devices is reduced to a level such that the device mobility is not greatly degraded by channel scaling.

The secondary objectives include the integration of *n*-channel and *p*-channel OFETs with comparable performance into complementary inverters, and finally the encapsulation of OFET devices and circuits, as also shown in Figure 1.3. With gate dielectrics and source/drain electrodes optimized for discrete *n*- and *p*-channel OFETs as stated in the primary objective, the integration of two types of OFETs is implemented by fabricating the devices on the same substrates with a combination of dielectrics and source/drain electrodes compatible with C_{60} and pentacene. By interface engineering of OFETs, the research achieves organic complementary inverters with a high-gain, a low operation voltage, good electrical stability (absence of hysteresis), and a high switching-speed. A multi-layer thin-film encapsulation method is used to protect the devices and circuits from moisture and oxygen using alternating layers of an inorganic oxide (Al_2O_3) and a polymer.

According to the motivations and objectives outlined above, the organization of the dissertation is structured as follows. Chapter 1 reviews the basic background in organic semiconductors and OFETs, as well as the literature on the progress in OFETs and organic complementary circuits. The current issues are also analyzed and described with

particular objectives identified. Chapter 2 introduces experimental details and methods regarding device structure and operation, device fabrication, and electrical characterization and testing in the area of OFETs. Chapter 3 presents the results pertinent to the interface engineering of pentacene *p*-channel OFETs with an emphasis on the dielectric surface modification and device operational stability. In addition to the effect of dielectric properties on device performance and stability, Chapter 4 also addresses the issue of high contact resistance in *n*-channel OFETs. With dielectric interfaces and electrodes optimized in Chapter 3 and Chapter 4, organic complementary inverters fabricated on a plastic substrate are finally demonstrated and the preliminary results from the encapsulation of inverters are also presented in Chapter 5. Chapter 6 summarizes the conclusions drawn from this study and presents recommendations for future work.

CHAPTER 2 EXPERIMENTAL METHODS

This chapter provides a detailed description of experimental methods used in this dissertation work. It starts with the illustration of device structures and operation, followed by the electrical characterization of OFETs. Four common device structures used in transistors are compared and different source/drain arrangements are explained. The operation of OFETs with a *p*-type semiconductor is systematically analyzed and illustrated. The current-voltage characteristics and the extraction of electrical performance in the linear and saturation regimes for OFETs are explained and the analytical method for evaluating contact resistance is introduced. The critical steps involved in the OFET fabrication are also presented, such as purification of organic semiconductors, preparation of gate dielectrics, and deposition of metal contacts. The last section of this chapter describes the experimental setup for the electrical characterization.

2.1 OFET Device Structures and Operation

2.1.1 Device Structures of OFETs

OFET device structures, determined by the position of the contacts (i.e., gate, source, and drain) relative to the organic semiconductor film, are similar to those of inorganic TFTs. The basic structures are either coplanar or staggered. The device cross-sections of the OFET test configurations are shown in Figure 2.1. They are simplified structures without considering individual device patterning. In a coplanar structure, also called bottom-contact structure, the gate, source, and drain contacts are all located on the same side of the organic semiconductor film, as shown in Figure 2.1(a) and (c). In a

staggered structure, also called top-contact structure, the gate contact is on the opposite side of the organic semiconductor film from the source and drain contacts, as shown in Figure 2.1(b) and (d). Each structure has two different configurations depending on the position of the gate contact, on the bottom side (bottom-gate or inverted) [Figure 2.1(a) and (b)] or the top side (top-gate) [Figure 2.1(c) and (d)] of the organic semiconductor film, respectively. Therefore, there are four basic device configurations based on the definitions above as summarized in Figure 2.1: (a) inverted-coplanar structure, (b) inverted-staggered structure, (c) top-gate coplanar structure, and (d) top-gate staggered structure.

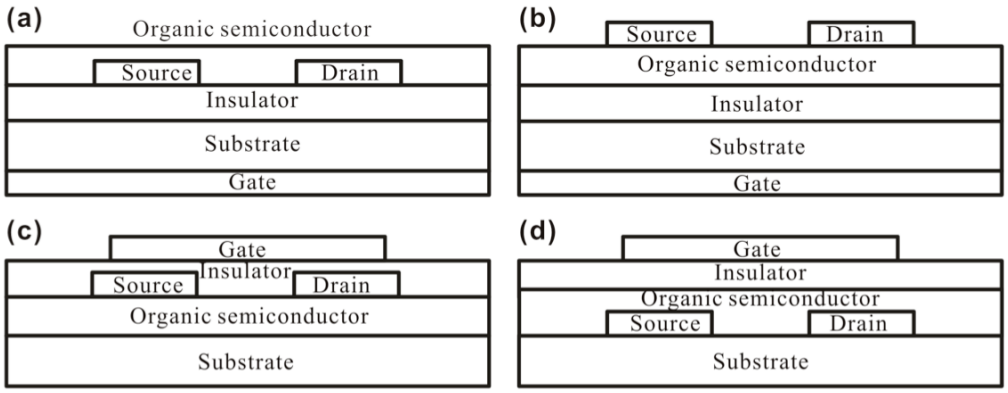


Figure 2.1: Cross-sections of simplified OFET device configurations: (a) Inverted-coplanar structure (bottom-contact); (b) Inverted-staggered structure (top-contact); (c) Top-gate coplanar structure; (d) Top-gate staggered structure.

Top-gate device structures as shown in Figure 2.1(c) and (d) have been applied to fabricate polymer TFTs [73, 74], but have not been widely used in the fabrication of OFETs. The electrical performance of OFET devices with a top-gate structure can be

significantly degraded during the deposition process of the top electrodes, and the film growth can be disturbed at the interface of organic semiconductor/metal contacts. The inverted-coplanar device structure as in Figure 2.1(a) is often referred as bottom-contact in the OFET literature and the inverted-staggered device structure as in Figure 2.1 (b) is often referred as top-contact in the OFET literature. In bottom-contact OFET devices, the organic semiconductor is deposited onto the gate insulator and source/drain contacts. In top-contact OFET devices, the source/drain contacts are usually deposited on the organic semiconductor through a shadow mask. To facilitate the evaluation of new organic semiconductor materials, heavily n-doped silicon (n^{++}-Si) wafer as the gate contact and thermal SiO_2 as gate insulator are used in these two structures.

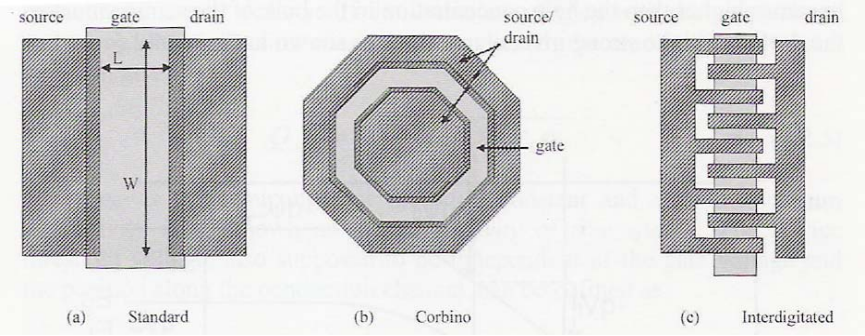


Figure 2.2: Top-views of OFET device structures: (a) Standard OFET; (b) Corbino OFET; (c) Interdigitated OFET [75].

Source/drain contacts are generally arranged in three ways (standard, corbino, and interdigitated) independent of device structure. The top views of these arrangements are shown in Figure 2.2. Typically, sources and drains in OFET devices are in direct contact

with the organic semiconductor and the semiconductor is not modified by the doping process used for inorganic metal oxide semiconductor field-effect transistors (MOSFETs). Similar to inorganic MOSFETs, the channel length of OFETs is defined as the geometrical separation between source and drain contacts and the channel width is defined as the geometrical width of the electrodes.

2.1.2 Device Operation of OFETs

The basic device operation can be explained using a bottom-contact OFET as an example, as shown in Figure 2.1(a). An OFET device can be considered as two capacitor plates separated by an insulator. One capacitor plate can be perceived as a conducting channel sandwiched between source and drain contacts, with the second plate of the capacitor located at the gate contact. The charge carrier density on this plate is modulated by the voltages applied to the three terminals: the source, the drain, and the gate.

To better understand how an OFET with such structure works, we first have to analyze its metal insulator semiconductor (MIS) structure. The energy level band diagrams of a MIS structure based on two different operation modes with a *p*-type organic semiconductor are shown in Figure 2.3.

Here an ideal MIS structure is assumed, which implies that the insulator is not conducting and the Fermi levels (E_F) of the metal and the semiconductor are aligned before contact. In other words, there is no band bending in the absence of external voltages, as seen in Figure 2.3(a). Here E_C is the lowest edge of the conduction band that corresponds to the LUMO level in organic semiconductors, and E_V is the highest edge of the covalent band that corresponds to the HOMO level in organic semiconductors. When a negative gate voltage (V_{GS}) is applied, the bands bend upward and the top of the HOMO

level moves closer to E_F, inducing an accumulation of the holes in the active channel near the insulator/semiconductor interface, as shown in Figure 2.3(b). When a positive gate voltage V_{GS} is applied, the bands bend downward, as seen in Figure 2.3(c), and the number of net charge carriers in the channel will decrease until the channel is fully depleted of free carriers. At this point, the electrons start to outnumber the holes, and the MIS structure is operated in the inversion region.

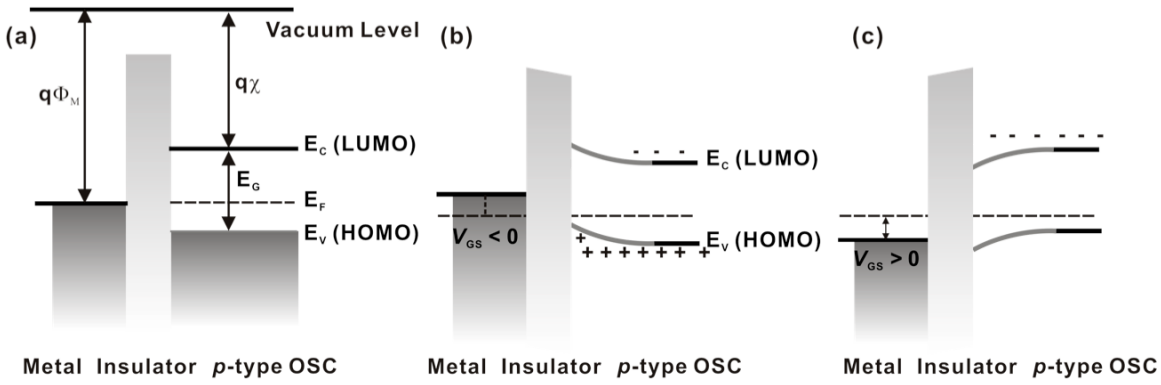


Figure 2.3: Energy level band diagram of an ideal MIS structure at equilibrium (a), biased in the accumulation region (b), and biased in the inversion region (c) for a *p*-type semiconductor.

OFETs differ from MOSFETs in their mode of operation: MOSFETs operate in the depletion or inversion mode, while OFETs (and inorganic TFTs) generally operate in the accumulation mode [76-79]. Since most OFETs exhibit a *p*-channel behavior within a *p*-type organic semiconductor, the following section will focus on the operation of OFETs with a *p*-type organic semiconductor in the accumulation mode.

The gate and the drain are both negatively biased and the source is grounded for a *p*-channel OFET within a *p*-type organic semiconductor, as shown in Figure 2.4. Positive

charges (holes) are injected from the source into the active layer (semiconductor), and then are accumulated at the semiconductor/insulator interface by the strong electric field across the insulator. The charges with opposite sign (electrons) are induced along the insulator/gate interface as in an ordinary capacitor. The newly formed charge carriers (accumulated holes at the semiconductor/insulator interface) generate a conducting channel between the source and the drain if their mobility is high enough and the charge carriers are not trapped. The accumulated charge carriers move (drift, hop, or tunnel) under the influence of the drain-source field and enter the drain. If the insulator has a capacitance per unit area, C_{OX}, then the accumulated charge density is simply $C_{OX}V_{GS}$, assuming that the voltage drop across the semiconductor and the insulator is negligibly small.

For a large negative gate bias and low drain bias, the accumulated charge carrier density is uniform throughout the conducting channel as seen in Figure 2.4(a). Assuming a constant mobility, the channel current increases linearly with the accumulated charge density $C_{OX}V_{GS}$ induced in the channel due to a voltage increase at the gate contact [79]. This is also characterized as a linear regime.

As the drain bias becomes increasingly negative, the voltage drop over the insulator and semiconductor becomes a function of the position in the channel as shown in Figure 2.4(b). At the source contact, the voltage drop and accumulated charge density will remain the same. At the drain contact the voltage drop decreases, giving rise to a lower accumulated charge density, and the accumulation charge density will decrease from the source to drain contact. If the drain becomes more negative than the gate then a depletion zone begins to appear and grow from the drain contact as shown in Figure 2.4(c). The

channel at the drain side is pinched off and the current increases sublinearly and even saturates. This is characterized as a saturation regime.

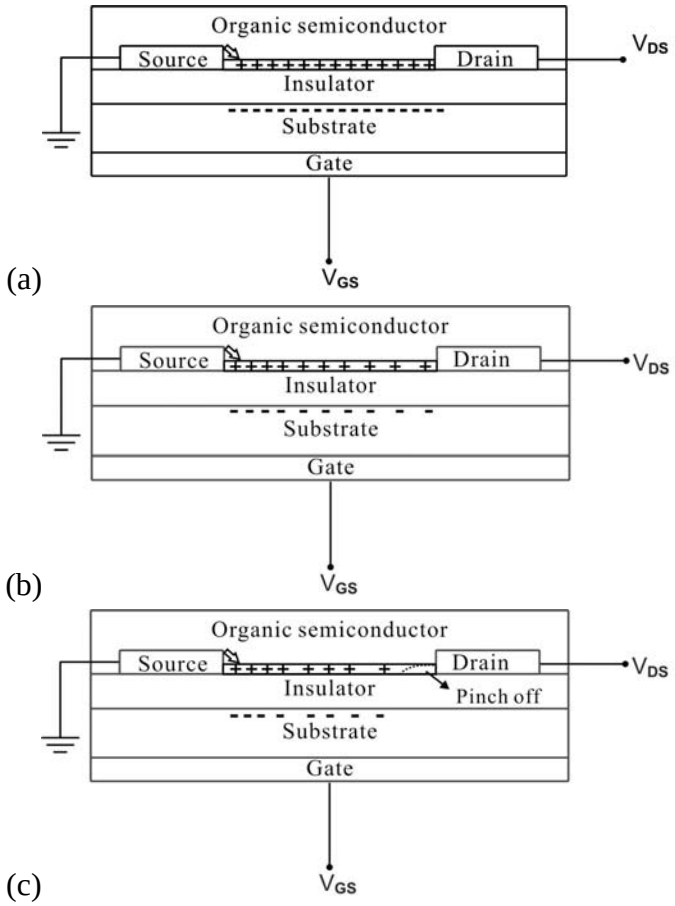


Figure 2.4: Schematic diagram of OFET operation. "+" represents a positive charge (hole) in the conduction channel, and "-" represents its opposite charge (electron). The schematic diagram describes the development of the positive accumulation region (a), non-uniform charge density in the channel (b), and the depletion region by the drain contacts (c), respectively. The arrow shows the injection direction of holes.

2.2 Electrical Characterization of OFETs

2.2.1 Current-Voltage (IV) Characteristics

Several analytic models have been developed to describe current-voltage characteristic in OFETs [76, 77, 79-81]. These models, based on the well-developed MOSFET model, usually incorporate the contact effect, field-effect mobility and other effects to account for non-linear effects in OFET characteristics. However, the parameters calculated and reported in the OFET literature are mostly extracted using expressions of drain current derived from traditional inorganic MOSFET model.

Using pentacene as an example, *p*-channel OFET operation can be described using a square-law model developed for MOSFET. The physical mechanism involved in device operational regions has been illustrated earlier in section 2.1. The regions are usually determined by the values of applied voltages V_{GS} and V_{DS} in the MOSFET modeling. As shown in Figure 2.5, the device is operated in the linear regime for $|V_{DS}| \leq |V_{GS} - V_T|$ and is operated in the saturation regime for $|V_{DS}| \geq |V_{GS} - V_T|$. Here, V_T is the threshold voltage.

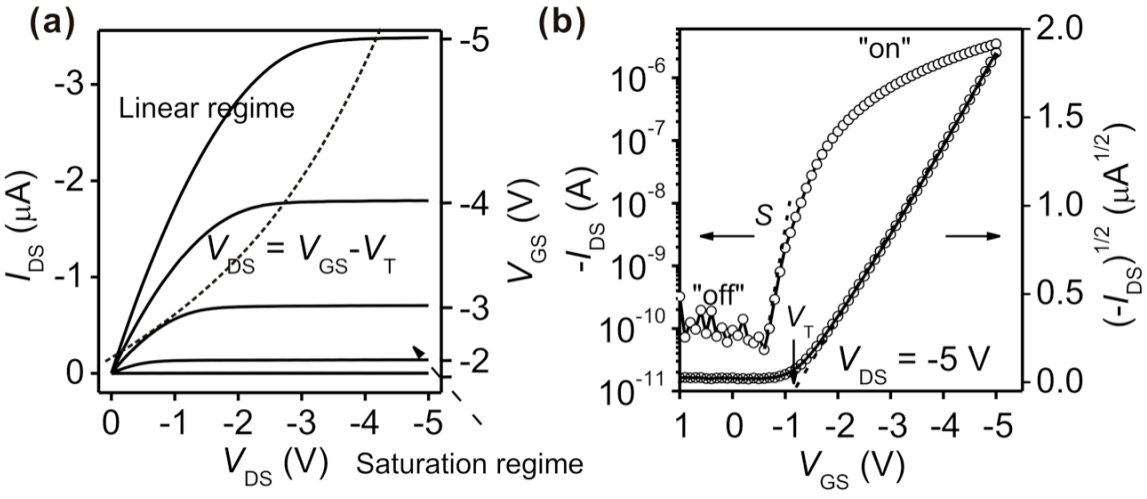


Figure 2.5: Typical electrical characteristic of a *p*-channel OFET device: (a) output curve and (b) transfer curve.

In the linear regime for $|V_{DS}| \leq |V_{GS} - V_T|$, the drain voltage V_{DS} is very low and the current varies linearly with it. The channel regime functions as a resistor and can be described as below:

$$I_{DS} = -\frac{W}{L} C_{OX} \mu [(V_{GS} - V_T) V_{DS} - \frac{V_{DS}^2}{2}] \quad \textbf{(1)}$$

For small V_{DS} ($|V_{DS}| << |V_{GS} - V_T|$), the second term in the square bracket can the ignored and Equation (1) can be simplified as:

$$I_{DS} = -\frac{W}{L} C_{OX} \mu [(V_{GS} - V_T) V_{DS}] \quad \textbf{(2)}$$

where W and L are the channel width and channel length, C_{OX} is the capacitance of the insulator, μ is field-effect carrier mobility, and V_{GS}, V_{DS} and V_T are the gate-source, drain-source and threshold voltages respectively. W (width) and L (length) are the dimensions of the semiconductor channel defined by the source and drain electrodes.

As drain voltage increases until $|V_{DS}|$ is larger than $|V_{GS} - V_T|$, the drain current becomes independent of the drain voltage and varies as the square of the gate-source voltage as shown in Equation (3). In this case, the device operates in a saturation regime.

$$I_{DS} = -\frac{W}{2L} C_{OX} \mu (V_{GS} - V_T)^2 \quad \textbf{(3)}$$

This model is based on the gradual channel approximation and assumes that the field-effect mobility is independent of the gate voltage, and that the source/drain contacts are ohmic [82, 83]. Therefore, the expression above does not account for the non-linear behavior of drain current at low drain bias generally observed in inorganic TFTs and OFETs.

2.2.2 Extraction of Electrical Parameters

Field-Effect Mobility μ and Threshold Voltage V_{TO}

The carrier field-effect mobility in the linear regime can be extracted from the transconductance g_m which is the change of I_{DS} with V_{GS} for a small drain voltage V_{DS}. From Equation (2), it is given by

$$g_m = -\frac{\partial I_{DS}}{\partial V_{GS}}\bigg|_{V_{DS}=smallconst.} = -\frac{W\mu C_{OX}}{L}V_{DS} \quad \textbf{(4)}$$

Therefore, the linear mobility μ solved from Equation (4) is given as:

$$\mu = -g_m \frac{L}{W}\frac{1}{C_{OX}}\frac{1}{V_{DS}}\bigg|_{V_{DS}=small\ const} \quad \textbf{(5)}$$

The field-effect mobility in the saturation regime is also extracted from the transfer characteristics (I_{DS} *vs.* V_{GS}) for the device biased as $|V_{DS}| \geq |V_{GS} - V_T|$. Equation (3) shows that the square root of the saturation current is linearly dependent on the gate voltage. The field-effect mobility can be extracted from the slope of the curve which plots the square root of the saturation current as a function of gate voltage V_{GS}, as shown in Figure 2.5(b). The mobility can be calculated from Equation (3) and is given as:

$$\mu = 2\frac{L}{W}\frac{1}{C_{OX}}\left(\frac{\partial\sqrt{I_{DS}}}{\partial V_{GS}}\right)^2 \quad \textbf{(6)}$$

I_{on}/I_{off}, Subthreshold Slope *S*, and Onset Voltage V_{TO}

Transfer characteristics (V_{GS} *vs.* I_{DS}) are often plotted on a logarithmic scale, as shown in Figure 2.5(b), which gives access to other important parameters, such as on-off

current ratio I_{on}/I_{off}, subthreshold slope S, and turn-on voltage V_{TO}. Note that the negative I_{DS} current is normalized in order to characterize it on a logarithmic scale.

I_{on}/I_{off} is the ratio of the maximum I_{DS} ("on" current) value to the minimum I_{DS} ("off" current) value, obtained from transfer characteristics plotted on a logarithmic scale. The ratio characterizes the ability of the device to switch a signal from "on" to "off". It also shows in Figure 2.5(b) that the subthreshold current starts increasing at V_{GS} = -0.5 V. The voltage at this point is defined as a turn-on or onset voltage V_{TO}. The physical meaning of this parameter has not been systematically investigated.

Subthreshold slope S is defined as the rate at which I_{DS} varies (in decades) with V_{GS} for device operation in the subthreshold region. It describes the turn-on characteristics of the device and is given as:

$$S = \frac{d|V_{GS}|}{d\log|I_{DS}|} \quad \textbf{(7)}$$

S can be extracted by fitting a line to the steepest part in the subthreshold region and calculating its inverse.

2.2.3 Schottky Contact and Calculation of Contact Resistance

Contact resistance is part of the total resistance (R) of the device, which limits the operation speeds due to charging, and discharging of the capacitor (C) associated with the device. Switching frequency of OFETs is expressed as $f \propto \frac{\mu V}{L^2}$ [60], where f is frequency, μ is mobility, V is applied voltage and L is channel length. High mobility in organic semiconductors and small feature size in device design are desirable to achieve high switching speed. However, device performance in short channel devices is typically

degraded due to the contact effect at the interface of metal/organic semiconductor [84-92]. Contact resistance in organic devices is much higher than that in amorphous TFTs, limiting the mobility of OFETs, therefore limiting the speed of organic integrated circuits. It is very important to understand the physical mechanism behind contact resistance and its relevance to the gate voltage, device structure, the properties of metal contact and organic materials, etc.

Two device structures, top-contact and bottom-contact, are usually applied in OFETs, as described in section 2.1. The contact effect is more pronounced in bottom – contact OFETs since there is a larger effective contact area in the top-contact configuration [84, 90], as shown in Figure 2.6. In the devices with a top-contact structure, no component of the applied electric field along the channel can induce injection/extraction from the top of the source contact, as shown in Figure 2.6(a), which may be the reason that OFETs with top contact structures are not sensitive to contact effect. In a bottom-contact OFET, there is a voltage drop across the contact area at the source contact due to contact resistance [Figure 2.6(b)], and it cannot be neglected compared to the voltage drop across the bulk active layer area.

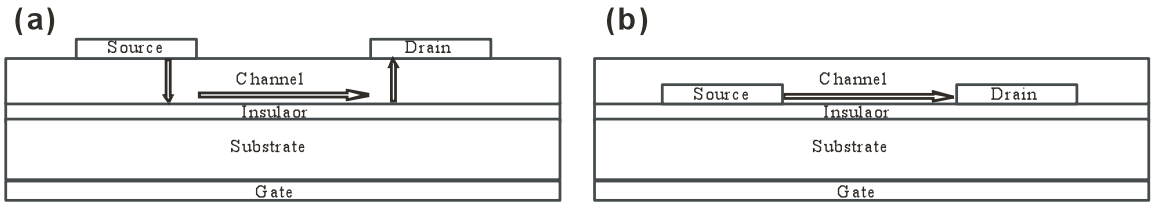


Figure 2.6: Schematic diagrams of top contact configuration (a) and bottom contact configuration (b). Arrows in the diagrams show the flow direction of current from high voltage (source) to low voltage (drain).

Generally, contact resistance originates from disturbed crystal growth at the edge of metal contacts and a contact barrier at the interface of the metal/organic semiconductor. The film at the edge of the contact is quite rough, and pentacene cannot form a well-defined terrace. Smaller crystal size at the edge forms a large number of grain boundaries that contain many morphological defects (e.g. void spaces). Those defects play a role as charge-carrier traps which is considered to be responsible for the degraded performance in bottom-contact pentacene OFETs [76].

Large contact barrier usually exists when injection or extraction of electrons occurs from the metal contact to organic semiconductor. Unlike in conventional MOSFETs, the metal contacts in OFETs cannot be modified by traditional doping methods, such as ion implantation, diffusion, etc. The barrier height depends on the HOMO and LUMO levels of the organic semiconductor relative to the work function of the metal. The voltage drop across the contact area cannot be negligible compared to the drop across the active region of the channel. For OFETs, the contacts are generally not ohmic, and the resistance associated with carrier injection and extraction is not the same. This has been confirmed using scanning potential imaging [93] and scanning Kelvin probe measurement [94]. The voltage drop was found larger at the source contact then at the drain for small-molecule OFETs with metal contacts biased in the linear regime. Figure 2.7 shows the presence of a barrier for hole injection from a metal contact (e.g. Au) into an organic semiconductor (e.g. pentacene) and a Schottky contact is formed at the interface of Au and pentacene.

Here, Φ_M is work function of metal, Φ_{Pc} is work function of the organic semiconductor, Φ_{Bh} is the barrier height at the contact, χ is the electron affinity, I_p is the ionization energy, and E_G is the energy gap which is determined by the position of

HOMO level and LUMO level. After contact, Fermi level E_F (given by the work function of the metal Φ_M) is aligned with the relevant carrier transport level of the organic semiconductor. The vacuum level is assumed constant.

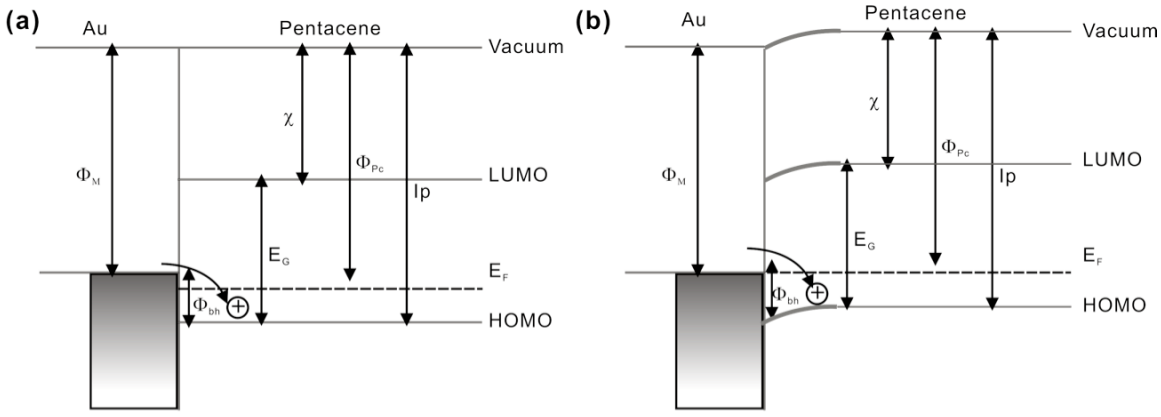


Figure 2.7: Energy band diagram for a Schottky contact before contact (a) and after contact (b) formed between Au contact and pentacene.

From Figure 2.7, the barrier height Φ_{Bh} can be calculated as

$$\Phi_{Bh} = E_G + \chi - \Phi_M \quad \textbf{(8)}$$

In addition, the work function of the organic semiconductor can be derived as:

$$\Phi_{Pc} = E_G + \chi - E_F \quad \textbf{(9)}$$

Therefore the band bending $\Delta\Phi$ is:

$$\Delta\Phi = \Phi_{Pc} - \Phi_M \quad \textbf{(10)}$$

The barrier height Φ_{Bh} between metal and pentacene was reported in the range of 0.5eV to 1.0 eV [95-97] and the barrier even exists between pentacene film and a noble

metal with a large work function (like gold Φ_M =5.2eV) which is close to the relevant conduction level (HOMO) of the organic semiconductor.

In this work, a top-contact configuration was employed to OFETs due to its lower contact resistance compared to that of OFETs with a bottom-contact configuration. As discussed earlier, the lower contact resistance in a top-contact configuration is associated with the increased effective contact area. On the other hand, the bottom-contact configuration is limited by the nonlinear film morphology near the contacts.

A schematic of OFETs in Figure 2.8 shows equivalent resistances corresponding to a source contact resistance (R_S), channel resistance (R_{Ch}), and drain contact resistance (R_D). The total contact resistance (R_S + R_D) is associated with carrier injection and collection at the source/drain contacts. The channel resistance R_{Ch} is associated with current crossing the channel length in the semiconductor.

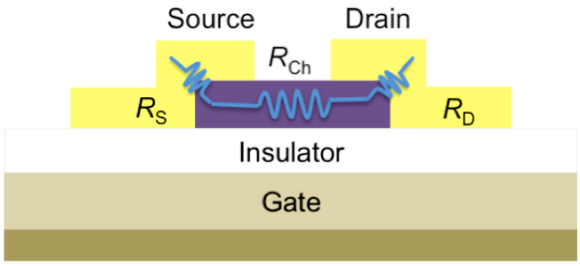


Figure 2.8: Schematic of OFETs showing equivalent resistances

In general, there are two contributions to contact resistance in top-contact OFETs: the resistance of the metal/organic interface (interfacial contact resistance), and the

excess resistance of the organic film itself where the charge carriers must travel from/to the S/D metal to/from the channel. The interfacial contact resistance is determined both by the injection barrier at the interface of the semiconductor and the source/drain contacts, and by the film morphology at the interface. The film access resistance is dependent on the thickness and the conductivity of semiconductor films.

The main factors that can lead to non-ideal contact resistances in organic semiconductor devices are energy level mismatch between the contact metal and semiconductor and disorder in the organic semiconductor layer at the semiconductor contact interface. Although one may choose a metal whose Fermi energy is well matched to the proper semiconductor band (in order to form an ohmic contact), there are complicating factors, such as interface dipoles at the metal-organic interface that may result in an energy level mismatch.

The extraction of contact resistances in is work follows a gated-transfer length method (gate-TLM) [also referred as a transmission line method (TLM)] empirical model that was applied to amorphous silicon TFTs developed by Luan and Neudeck [98] and Rolland [99]. Recently this model has been applied to extract the contact resistance from polymer-based OFET devices with bottom contact polymer electrodes [84], organic transistors that use soft contact laminated contacts [91], poly(3-hexylthiophene) field-effect transistors [100], pentacene transistor printed on PANI/SWNT [88], and pentacene transistors with top contact evaporated gold electrodes [90].

The contact resistance of OFETs can be extracted using a transmission line method (TLM) based on the dependence of current-voltage characteristics on channel length. In

the linear regime, the overall device resistance R_{on} can be considered as the sum of the channel resistance R_{ch} and a total contact resistance R_C according to [99]:

$$R_{on} = \frac{\partial V_{DS}}{\partial I_{DS}}\bigg|_{V_{DS}\to 0}^{V_{GS}} = R_{ch} + R_C = R_{sh}\frac{L}{W} + R_C \quad \textbf{(11)}$$

$$R_{on}W = R_{sh}L + R_C W \quad \textbf{(12)}$$

$$R_{sh} = \frac{1}{\mu_c C_i (V_{GS} - V_{Ti})} \quad \textbf{(13)}$$

where $R_{sh,}$ μ_c, and V_{Ti} are the sheet channel resistance, the corrected mobility and threshold voltage, respectively.

According to Equation (12) and (13) , the total width-normalized contact resistance ($R_C W$) can be extracted by plotting the width-normalized total resistance ($R_{on}W$) as a function of L for different gate voltages. By extrapolating $R_{on}W$ to L = 0 μm, the y intercept of the least squares fit yields $R_C W$ and the slopes correspond to the sheet channel resistance R_{sh}.

According to Equation (13), a corrected mobility (μ_c) from the contact resistance can be calculated from the slope of the linear least-square fit of R_{sh}^{-1}, which is equivalent to the channel sheet conductance.

2.3 OFET Fabrication

2.3.1 Purification and Deposition of Organic Semiconductors

Charge carrier transport in organic semiconductors is known to be sensitive to the presence of chemical impurities [101]. It is generally acknowledged that higher purity correlates with higher performance and contributes to device reproducibility and stability.

The impurities result in molecular defects and trapping states in crystals or thin films, which impedes the electronic transport. For example, impurities like pentacene dimers and quinone usually exist [102]. While traditional solution-based purification methods such as distillation and liquid chromatography may remove impurities at the sub-percent level, a much higher level of purity is required to achieve for electronic transport in semiconductors. In fact, impurities present even at the part-per-million level are known to have a large effect on transport in inorganic semiconductors [103]. The most common approach is a variation of thermal-gradient sublimation, often termed physical vapor transport, performed under reduced pressure and/or flowing inert gas.

In this work, each oligomer was purified by thermal gradient zone sublimation using a three-temperature-zone furnace (Lindberg/Blue Thermo Electron Corporation) as shown in Figure 2.9. This technique involves heat-induce sublimation of starting material and the subsequent condensation in a separate temperature zone under a vacuum level of approximately 10^{-6} Torr. Each material has a particular sublimation point: heavier materials sublimate at higher temperatures and light materials at lower temperature. This results in an extra degree of refinement in the crystallization process.

The temperature gradient is tuned to sublimate the light, high-vapor-pressure impurities and the materials desired from the source, and keep the heavy, low-vapor-pressure impurities in the crucible. The sublimed material then condenses on the cooler walls in the low temperature zone. This method separates, in the vapor phase, pure material from lower-molecular-weight (i.e., higher-vapor-pressure) impurities that travel farther down the process length, and higher-molecular-weight (i.e., lower-vapor-pressure) impurities that remain at or near the source material.

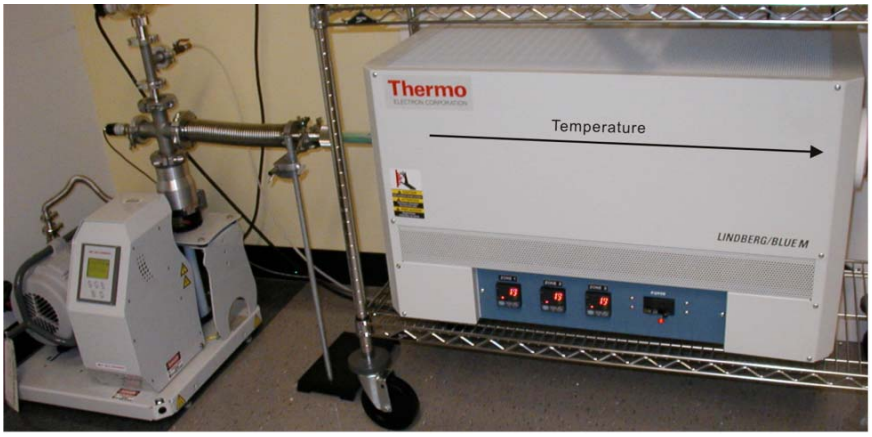


Figure 2.9: A three-temperature-zone furnace from Lindberg/Blue Thermo Electron Corporation.

Parameters important to the purification of pentacene (Sigma-Aldrich) and C_{60} (Alfa Aesar) are as follows. For pentacene, the thermal gradient was adjusted so that the hottest zone was about 250-270 °C, the middle zone at around 184 °C, and the final zone at around 164 °C. For C_{60}, the thermal gradient was adjusted so that the hottest zone was about 540 °C, the middle zone at around 425 °C, and the final zone at around 334 °C. The heavy impurities are left in the hottest zone while the light impurities are left in the coolest zone. The final purified compounds are collected from the middle zone.

The deposition processes are performed through a computer controlled physical vacuum deposition (PVD) system called SPECTROS manufactured by Kurt J. Lesker Company (KJLC). The system is specifically designed to investigate the deposition methods and characteristics of organic and polymeric materials for novel organic electrical and electro-optics devices. The configuration of the SPECTROS system is shown in Figure 2.10.

Figure 2.10: KJLC's computer controlled SPECTROS PVD system.

This system is equipped with four organic and two metal sources and has a capability to carry out co-depositions of several materials. In our application, other than the controller part, the SPECTROS system is accessed via a N_2-filled glovebox from MBRAUN Company in order to handle oxygen and water sensitive organic materials. The deposition condition (substrate temperature, deposition rate, and base pressure, film thickness, etc) for individual materials is written into a recipe and the deposition process is automatically programmed and executed. The chamber is pumped by a cryopump with roughing and regeneration provided by a rotary vane pump.

The thin films are obtained using a thermal evaporation controller in a high-vacuum environment with a base pressure lower than 10^{-7} torr. The sample is fixed on a substrate holder with a shield mask at the top to form patterns of the active layer onto the sample. Pre-purified material is loaded into an organic source designed for low temperature evaporation (up to 500ºC) with a pneumatically actuated shutter. Deposition

rates are monitored by standard quartz crystal monitors. The film thickness is controlled by a substrate sensor controller. Deposition conditions, such as deposition rate and substrate temperature, film thickness, have a significant influence on the ordering and the packing of the molecules, and the morphology of the organic films. In the experiments presented in this work, pentacene or C_{60} of 400-600 Å is thermally evaporated at a rate of 0.3-1 Å/s onto OFET substrates held at room temperature.

2.3.2 Preparation of Gate Dielectrics and Interfacial Control

Preparation of Gate Dielectrics by Atomic Layer Deposition

To achieve high performance OFETs, development of suitable gate dielectric materials is always important in addition to high-mobility organic semiconductors. Preferably, dielectric materials should have a high dielectric constant (κ) and should be processible into thin, high quality, and defect-free films to form OFETs with a reduced operating voltage, fast switching speed, and large on/off current ratio. Low deposition temperature is desirable to allow for fabrication on plastic substrates. Atomic layer deposition (ALD) is a deposition technique that allows for the deposition of highly conformal, defect-free dielectric layers at relatively low temperature [104-107]. Dielectric films grown by ALD have a high resistivity and good barrier properties, and therefore are excellent candidates for gate insulators. This deposition process is simple, low-cost, and compatible with various substrates made from different materials and with irregular shapes [104, 105]. Oxide layers fabricated by ALD have also been studied as O_2/H_2O barriers for organic light-emitting diodes [108]. However, to date ALD technology has had limited success in fabricating dielectric materials suitable for OFET applications [109, 110].

Except as specially mentioned, most devices and circuits in this dissertation were fabricated on heavily n-doped Si (n^{++}-Si) wafers as both the substrates and gate electrodes. Some transistors were fabricated on ITO-coated glass to investigate the effectiveness of the gate dielectrics on rough substrates. At the end of the dissertation, fabrication of organic complementary circuits is explained. The organic circuits were fabricated on plastic substrate to demonstrate the advantage of organic electronics.

The ALD cycle for Al_2O_3 deposition is illustrated in Figure 2.11 and the chemical reactions are described in Figure 2.12. The cycle for Al_2O_3 deposition is demonstrated with silicon wafers as substrates. Under normal atmosphere, H_2O vapor is adsorbed on Si surface, forming hydroxyl groups Si-O-H with silicon. Plasma treatment with O_2 for short time can also be used to induce a uniform layer of hydroxyl groups on the surfaces. The deposition process involves alternate exposure of two precursors to the substrate surface. First, precursor trimethylaluminum (TMA) is pulsed into the reaction chamber and reacts with the adsorbed Si-OH groups until the surface is fully occupied or passivated. The reaction is terminated to one layer since TMA does not react with itself. The excess TMA is pumped away with the reaction product, in this case, methane. Then H_2O vapor is pulsed into the reaction chamber to react with the dangling methyl groups on the new surface, forming aluminum-oxygen (Al-O) bridges and hydroxyl surface groups and waiting for a new TMA pulse. The excess H_2O vapor and reaction product methane are pumped away. Excess H_2O vapor does not react with the hydroxyl surface groups, again causing perfect passivation to one atomic layer. This completes one cycle with a thickness of approximately 1 angstrom. The cycle can be repeated multiple times to achieve a desired thickness.

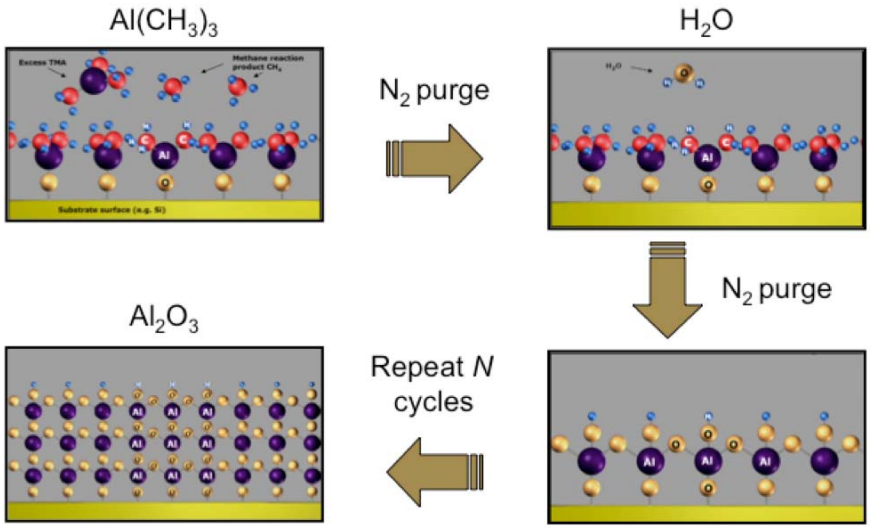


Figure 2.11: ALD example cycle for Al_2O_3 deposition (Cambridge NanoTech Inc.)

$$Al(CH_3)_{3(g)} + :Si-O-H_{(s)} \rightarrow :Si-O-Al(CH_3)_{2(s)} + CH_4$$
$$2H_2O_{(g)} + Si-O-Al(CH_3)_{2(s)} \rightarrow :Si-O-Al(OH)_{2(s)} + 2CH_4$$
$$Al(CH_3)_{3(g)} + :Al-O-H_{(s)} \rightarrow :Al-O-Al(CH_3)_{2(s)} + CH_4$$
$$2H_2O_{(g)} + :O-Al(CH_3)_{2(s)} \rightarrow :Al-O-Al(OH)_{2(s)} + 2CH_4$$

Figure 2.12: Chemical reactions for Al_2O_3 deposition in an ALD process.

Interfacial Control at the Gate Dielectric/Semiconductor

In addition to the influence of deposition conditions on the growth and morphology of organic semiconductors, it is well established that a chemical treatment of the gate dielectric surfaces with self-assembled monolayers (SAMs) can significantly change the surface energy, therefore facilitating the formation of an orderly structure in organic films grown on top, especially for the first monolayer. It has been shown that the charge transport often occurs in the first few monolayers of the semiconductor film. The

beneficial effects of the surface treatment are also attributed to the fact that SAMs can passivate the charge trapping species on the dielectric surface, such as SiOH groups at the SiO_2 surface as electron-trapping sites.

Silane-based SAMs can react with SiO_2 surface and form dense, well-ordered, and uniform monolayers. The end groups can be tailored to be favorable to the semiconductor molecules and charge transport. Among them, octadecyltrichlorosilane (OTS), a SAM with long alkane chains, have demonstrated the best results. The chemical reactions of OTS molecules on SiO_2 are described in Figure 2.13 (a).

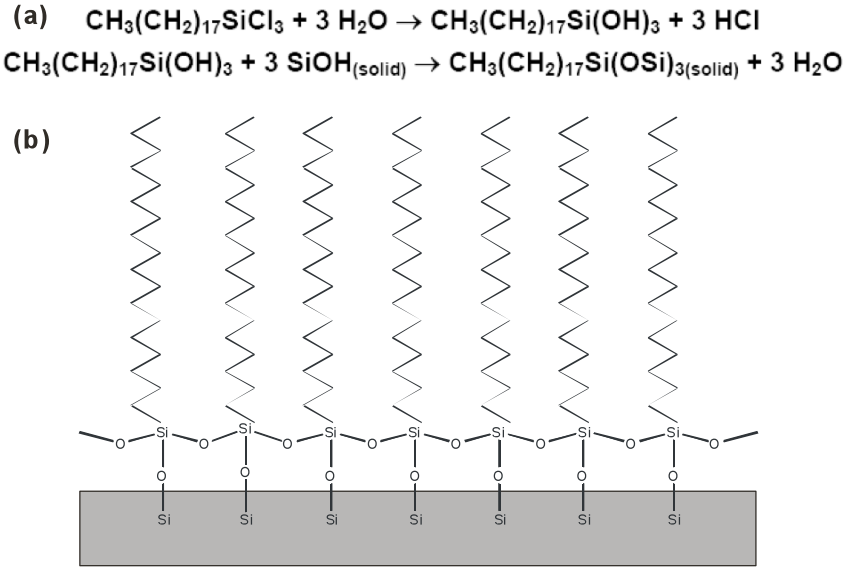


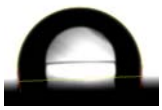
Figure 2.13: A schematic view of OTS molecules binding on SiO_2.

An OTS molecule, $CH_3(CH_2)_{17}SiCl_3$, can hydrolyzed with three water molecules into $CH_3(CH_2)_{17}Si(OH)_3$ possessing three Si-OH groups. The generated

$CH_3(CH_2)_{17}Si(OH)_3$ can react with SiOH from other OTS molecules or on SiO_2 surface. In a well-controlled manner, the reaction will bind OTS to the SiO_2 surfaces and condense to siloxanes (Si-O-Si). An extended monolayer network will form through interchain crosslinking of OTS, as shown in Figure 2.13 (b).

To obtain uniform, smooth, and high-coverage OTS SAM layers, it is critical to have proper substrate preparation, impurity-free OTS and solvent, humidity control, and reaction time. In addition to the removal of particles and organic contaminants, the substrate preparation also prefers a pre-treatment of surfaces to create dense Si-OH groups. Oxygen plasma treatment is a simple and convenient means to achieve this purpose. The effect of treatment was demonstrated by the contact angle with DI water and final thickness, as shown in Table 1.

Table 1: The thickness and contact angle of OTS SAM with and without oxygen plasma treatment.

	No plasma O_2	Plasmas O_2 (15s)	Plasmas O_2 (2min)
Thickness	1.769 nm	2.067 nm	2.26 nm
Contact angle with DI water Before/After	 ~40 º / 98.5 º	 ~0 º /99.7 º	 ~0 º / 102.1 º

The substrates were well-cleaned Si wafers with a layer of native oxide (thickness: 1.776 nm). With plasma treatment, the oxide surface was occupied with dense Si-OH groups and the surface became hydrophilic with water contact angle decreasing from 40°

to 0°. With the plasma treatment time longer than 2 min, a thickness around 2.26 nm is formed, which is similar to the calculated OTS length 2.275 nm at the same orientation [111]. To avoid the high reactivity of chloride groups in OTS with water molecules, the treatment was carried out in a N_2-filled glovebox using anhydrous toluene or hexane as solvent at a very low concentration of 5-10 mM for several hours. After treatment, an immediate rinse with solvents, sometimes with short-time ultrasonication, can remove the physically absorbed OTS molecules. The subsequent baking in a vacuum oven can further remove water residues or uncrosslinked OH groups.

In the case of the surface treatment for Al_2O_3 surfaces, the acidicity of the OTS solution in a dry environment is so low that the slow etching of Al_2O_3 can be eliminated. Therefore, silane-based OTS was also selected to modify the Al_2O_3 surface and compare with SiO_2 even though phosphoric acid based SAMs are reported preferred for Al_2O_3 surfaces [43].

The concept of surface modification with SAM molecules can be extended to the usage of thin polymeric layers. The polymeric surface treatment can be applied by spin coating from a low-concentration solution of the polymer in organic solvents. As compared to SAMs, this straightforward method can provide an efficient surface passivation layer with excellent uniformity and full coverage. With a thin poly (α-methylstyrene) (PS) as a surface modification layer on the gate dielectric surface, a mobility as high as 7 cm^2 /V s with thin film pentacene transistors was demonstrated by 3M [19]. This method works especially well for *n*-channel OFETs since electron transport is very sensitive to the trapping site on the dielectric surface, which cannot be fully passivated by SAMs. Furthermore, the polymeric layer can also reduce the

roughness of the surface, which can disturb the growth of the organic layer and charge transport at the interface.

In this dissertation, three hydroxyl-free polymer compounds were selected to provide a good passivation layer on oxide surfaces and their chemical structures were shown in Figure 2.14. The three hydroxyl-free polymers are divinyltetramethyldisiloxane-bis(benzocyclobutene) (BCB) (Cyclotene^{TM}, Dow Chemicals), polystyrene (PS), and poly (methyl methacrylate) (PMMA). The thin films from diluted Cyclotene^{TM} BCB (with mesitylene) were crosslinked at 250 ºC on a hot plate for 1 hour in a N_2-filled glovebox. PS or PMMA films were spin-coated from a 4 mg/ml solution in toluene and annealed at 130 ºC on a hot plate for 1 hour.

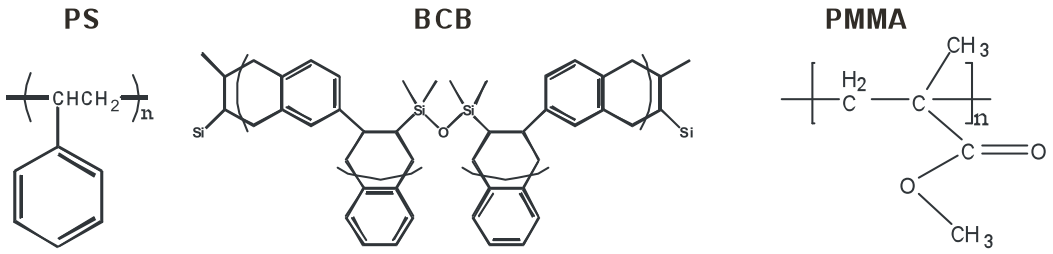


Figure 2.14: Chemical structures of PS, BCB, and PMMA.

2.3.3 Patterning and Deposition of Metal Contacts

As discussed earlier, the contact resistance can be greatly reduced in a top-contact configuration where source/drain electrodes are deposited directly on top of the organic semiconductor. Gentle patterning methods, such as printing and shadow masking

methods, can cause the least damage to the structural ordering of the organic semiconductor. Printing methods show great potential to provide low-cost and high resolution patterning, but it also involves chemicals and drying processes that often degrade the performance. Hence, shadow masking has been used as a production method for patterning organic layers in many OLED devices even though it has limited resolution and complexity. Similar types of masks, with more complicated patterns, can be used to fabricate circuits in a variety of materials [112].

The simplest types of masks are often cut from metal foil or thin sheets, using machining tools, electroplating and etching. Metal masks are inexpensive, commercially available, and easy to use. Their disadvantages are that they often have sharp/rough edges that can damage deposited thin layers, as shown in Figure 2.15. Silicon shadow masks can be very thin, flat, and precise since they can be fabricated using traditional photolithography and well-known deep-etching methods. However, the silicon masks are very fragile, and the size is limited by the capability of lithography. Polymeric aperture masks have been used by several groups in processing complex organic circuits with reduced damage to previously patterned layers [19, 43]. Polymer shadow masks can be made by using excimer laser ablation with high precision and accuracy. Some researchers have been able to show very small feature sizes also using shadow masks [113].

In this work, the commercially available shadow masks with a minimum channel length of 25 μm were used to pattern the discrete transistors. The patterning of complementary circuits used a set of shadow masks cut by an excimer laser at the Georgia Institute of Technology and the minimum channel length is 70 μm. Physical vapor deposition (PVD) was preferred for the deposition of metal due to less risk and low

cost. Both a thermal evaporator and an Electron-beam (e-beam) evaporator, available in our laboratory, were used for the deposition of metals.

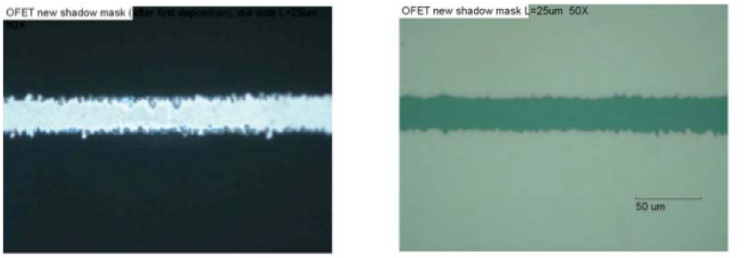


Figure 2.15: Optical images of shadow mask and its pattern on the poly(vinylphenol) (PVP) substrate.

2.4 Setup of Electrical Characterization

All the electrical measurements are carried out in an MBraun Labmaster 130 N_2-filled glovebox (H_2O, O_2 < 0.1 ppm) with a Lucas-Signtone H100 series probe station in a dark environment. The current-voltage characterization was mainly conducted with an Agilent E5272A 2 channel source-monitor unit (± 100 V dc range, 200 mA current limits). The illustration of the experimental set up along with an OFET device under test is shown in Figure 2.16. The capacitance–voltage characterization was performed with an Agilent 4284A precision LCR meter (20 Hz to 1 MHz) while the breakdown voltage was applied using a Keithley 248 High Voltage Supply. For the dc characterization of complementary inverters, in addition to Agilent E5272A SMUs, a dc Output Power Supply (Agilent E3647A) was used to apply the supply voltage V_{DD}.

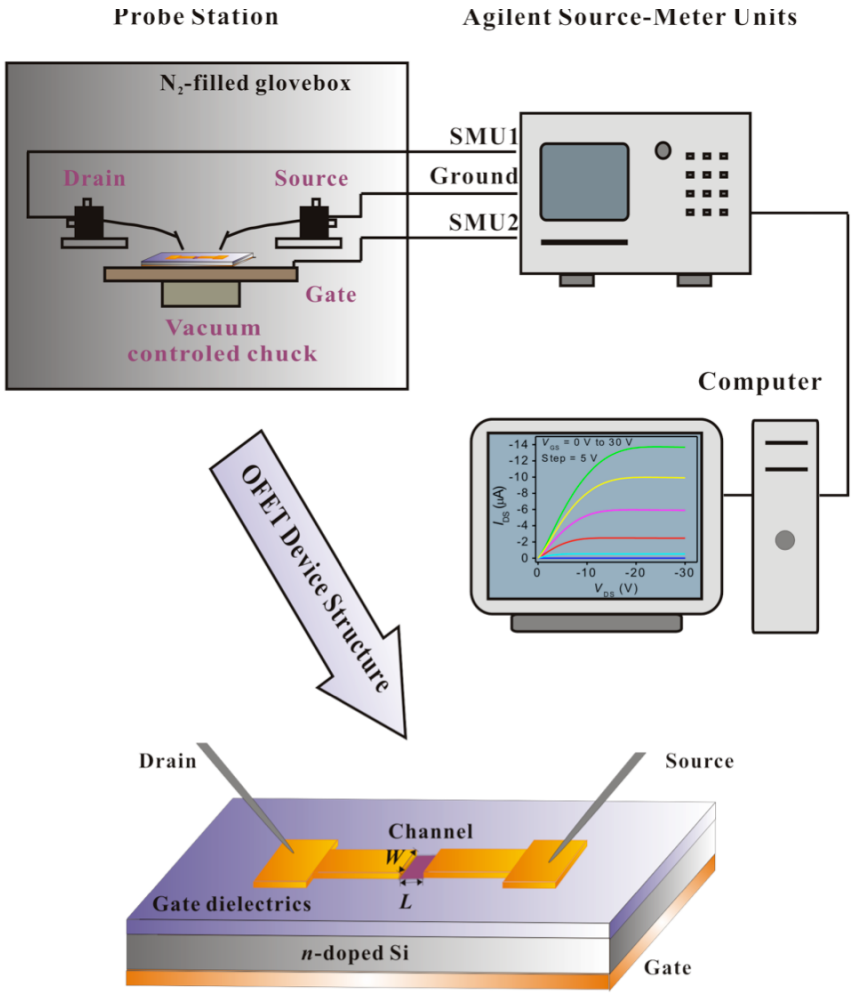


Figure 2.16: Experimental set-up and device structure under test.

The probe station consists of micromanipulators that can move probes in three axes and a linear translation stage positioned on a portable air table to lower the vibration. The shielded/guarded cables and wires are connected from the probe station to the equipment through the electrical feedthroughs on the glovebox. For the devices with a backside common gate, the samples are connected by a gate chuck connected to a source meter by shielded coaxial cables. All measurements and data acquisition are automated using

customized National Instruments LabView codes running on a GPIB-connected windows-based computer. Programs, like Originlab, Matlab, and Office Access are used for data analysis. AutoCAD and Coreldraw are used for mask design and drawing.

CHAPTER 3 P-CHANNEL PENTACENE OFETS

3.1 Pentacene OFETs with Al_2O_3 Gate Dielectrics Prepared by ALD

This section focuses on the fabrication of high-performance pentacene OFET devices with Al_2O_3 grown by ALD as the gate dielectric material. It starts with characterizing the dielectric and the surface properties of Al_2O_3 thin films. The OFETs were fabricated on heavily n-doped silicon (n^{++}-Si) substrates (serving also as the gate electrode) with 200 nm-thick films of Al_2O_3 grown by ALD as the gate dielectrics. A 200 nm-thick film of thermally grown SiO_2 was used as a reference control sample. Finally, we used the conformal aspect of ALD to fabricate high performance OFETs on a substrate with a large surface roughness: an indium tin oxide (ITO) coated glass substrate.

3.1.1 Deposition and Characterization of Al_2O_3 Gate Insulators

A Savannah100 ALD system from Cambridge Nanotech Inc. was used to deposit Al_2O_3 dielectric films on n^{++}-Si substrates (5×10^{-3} Ω-cm) and on ITO-coated glass substrates (Colorado Concept Coatings, 60 Ω/sq.). ITO-coated glass substrates were cleaned in an ultrasonic bath using, successively, soapy water, deionized water, acetone, and reagent alcohol for 15 minutes each, and then dried under nitrogen. The n^{++}-Si substrates were cleaned in a mixture of H_2SO_4/H_2O_2, and a buffered oxide etchant (1:6 diluted HF in H_2O) was used to remove the natural oxide. Immediately before being loaded into the ALD deposition system, the substrates underwent O_2 plasma treatment in a plasma asher for 10 minutes at low power. This plasma treatment is known not only to remove organic residues and other contaminants from surfaces, but also to increase the

concentration of surface hydroxyl groups and the amount of absorbed aluminum precursor [114]. Al_2O_3 films were deposited at 100 °C using alternating exposures of $Al(CH_3)_3$ and H_2O vapor at a deposition rate of approximately 1 Å per cycle. Each deposition cycle (one monolayer) lasted 24 s, yielding a total deposition time of 13.3 hours for 2000 cycles. The thickness of the Al_2O_3 films was measured by a stylus profilometer (Dektak 6M by Veeco) and found to be 200 nm.

We characterized the dielectric properties of 200 nm-thick Al_2O_3 films grown on ITO-coated glass using parallel plate capacitors of various plate areas ranging from 3.1×10^{-3} cm^2 to 2.4×10^{-1} cm^2. The capacitors were fabricated by sandwiching the Al_2O_3 film between an ITO electrode and a 100 nm-thick Al electrode. For each of the 12 devices, capacitance and dissipation factor (loss tangent) were measured at 1.0 V_{RMS} as a function of frequency from 20 Hz to 1 MHz with an Agilent 4284A precision LCR meter. The dielectric constant (κ) of Al_2O_3 at 1 kHz was determined to be 7.5 ± 0.2 (calculated from the linear dependence of capacitance as a function of device area $C_{OX} = \frac{\varepsilon_o k}{t}$, where ε_o is the permittivity in vacuum, t is the thickness, and κ is the dielectric constant). This result is comparable to the value obtained by Groner [105]. The current density vs. voltage characteristics presented in Figure 3.1(a) shows that a 200 nm-thick Al_2O_3 film is an excellent insulator with a leakage current density less than 200 nA/cm^2 under an applied field of 2 MV/cm over a contact area of 0.016 cm^2. Notably, these values are small considering the large surface roughness of ITO-coated glass. Dissipation factors for all devices were measured in the range of 10^{-3}. Furthermore, the capacitance density C_{OX} was stable up to a relatively high frequency of 1 MHz, as shown in Figure 3.1(b).

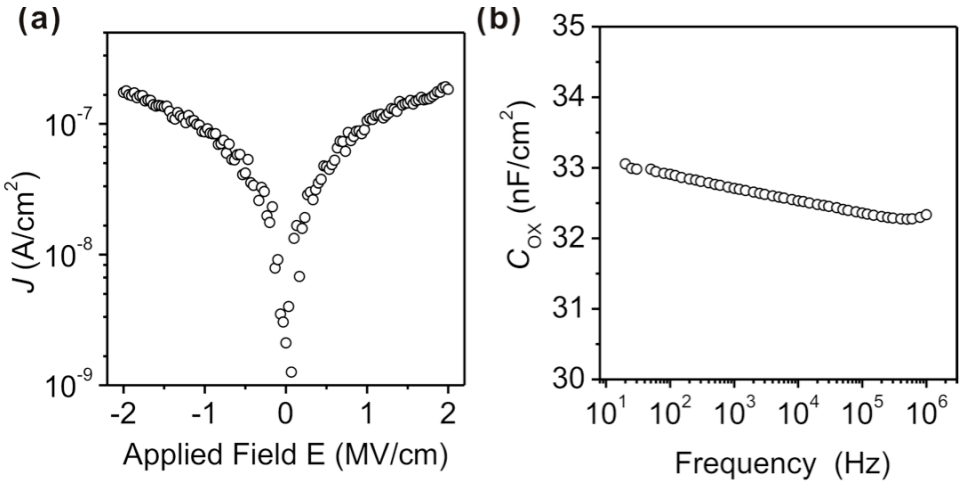


Figure 3.1: Current density (*J*) vs. applied field (E) characteristics (a) and capacitance density (C_{OX}) vs. frequency characteristics (b) of capacitors prepared with ALD grown Al_2O_3 dielectric materials on ITO-coated glass substrates.

In addition to dielectric properties, the chemical and physical surface properties of dielectrics, including surface wetting properties, surface roughness, and surface defect density, are also important parameters that affect the electrical performance of OFETs, through the morphology/structural ordering of organic semiconductor films and the charge transport at the dielectric/semiconductor interface. To characterize the surface properties, first, an element analysis of Al_2O_3 films was done by energy dispersive spectrometry (EDS). No elements other than Al, O, and elements from the substrates (e.g., Si, In, and Sn) were detected over a test area of 10 μm × 10 μm. Then, the surface morphology of Al_2O_3 on both n^{++}-Si substrates (smooth) and on ITO-coated glass (rough) was investigated by AFM (Digital Instruments NanoScope™ Scanning Probe Microscopes). The results were compared with thermally grown SiO_2 on n^{++}-Si substrates as shown in Figure 3.2. The root-mean-square (*rms*) surface roughness of the 200 nm-thick Al_2O_3 film on an n^{++}-Si substrate was estimated to be 4.3 Å when measured over an

area of 1 μm × 1 μm, which is almost identical to that of the 200 nm-thick SiO_2 film thermally grown on an identical n^{++}-Si substrate (4 Å). With an ITO-coated glass substrate, the *rms* surface roughness of Al_2O_3 films was increased up to 12 Å, which is comparable to the value of the substrate prior to deposition.

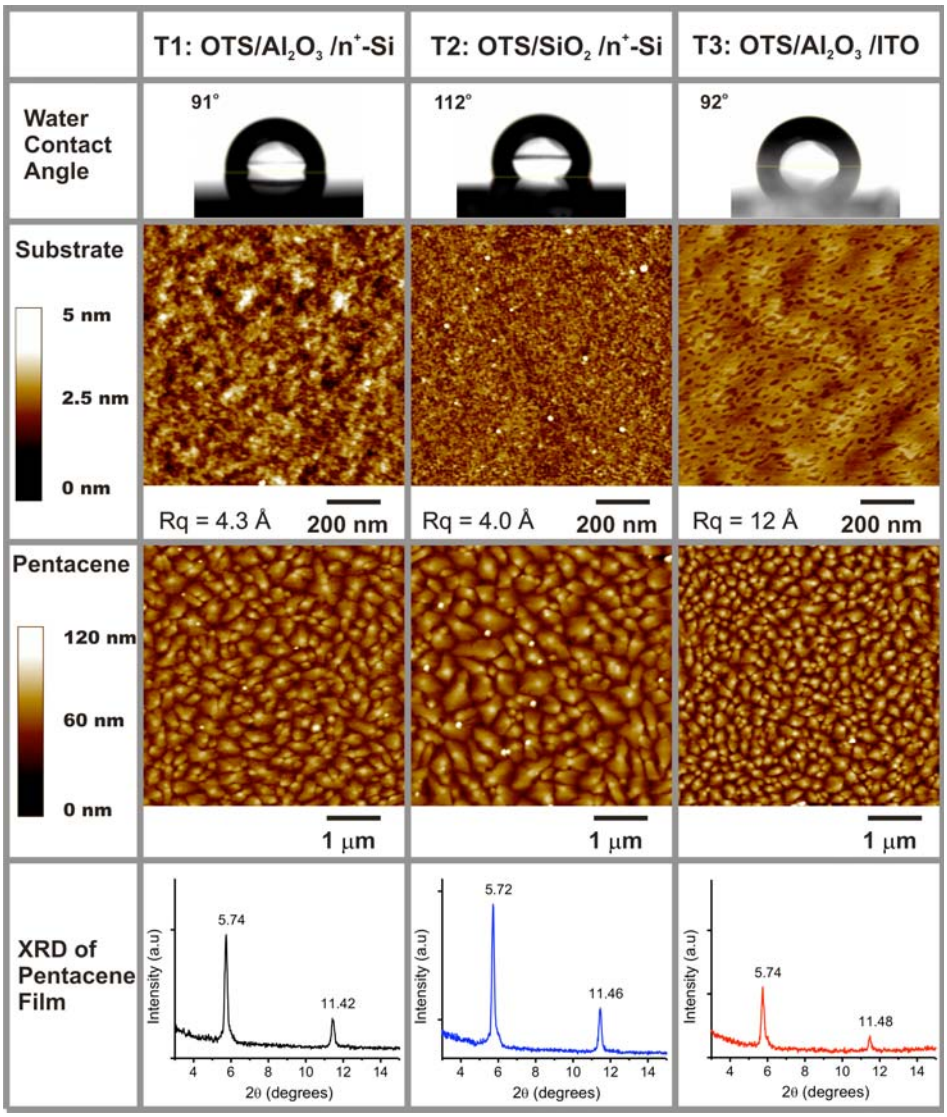


Figure 3.2: AFM images and water contact angles of substrates and pentacene morphology (i.e., AFM and XRD) on the substrates.

So far, we have obtained high-quality Al_2O_3 dielectric insulators with a dielectric constant (κ = 7.5) almost twice that of SiO_2. Although high-κ dielectric insulators are desirable for reducing operating voltage of OFETs, Veres [115, 116] has reported that high-κ dielectrics usually contain polar functional groups that can increase the energetic disorder at the interface, which results in a higher localization of the charge carriers and reduced field-effect mobility in polymer OFETs. Recent studies based on organic single-crystal transistors have attributed the dependence of mobility on dielectric polarizability to the coupling/interaction force between the charged carriers in the organic conducting channel and the ionic lattice of the dielectric [117, 118]. To minimize the effect of dielectric polar functional groups and other surface charges on the organic conducting channel, the surfaces of all oxides were passivated with an octadecyltrichlorosilane (OTS) self-assembled monolayer (SAM) before the deposition of pentacene. It is well established that SAMs applied on the interfaces in OFETs allow for better control of the morphology and properties of the organic semiconducting material. The OTS SAMs were formed by dipping the substrates in a 5 mM toluene solution of OTS for 30 minutes after the substrates were oxygen-plasma treated for two minutes. The static aqueous contact angle measurement showed that after the treatment, the previously hydrophilic surfaces of both dielectric materials became hydrophobic. A contact angle of 91°- 92° was obtained from OTS-treated Al_2O_3 on both smooth surface (n^{++}-Si) and rough surface (ITO-coated glass), indicating that a uniform self-assembled OTS monolayer with long alkyl chains was formed. This value is slightly lower than that of OTS-treated SiO_2 on n^{++}-Si (112º). This can be attributed to a lower concentration of oxygen atoms of Al_2O_3 and a different SAM formation mechanism compared with SiO_2 [119, 120].

3.1.2 Fabrication and Characterization of OFETs with Al_2O_3 Gate Insulators

OFETs were fabricated using 200 nm-thick Al_2O_3 on n^{++}-Si (T1), 200 nm-thick SiO_2 on n^{++}-Si (T2, the reference sample), and 200 nm-thick Al_2O_3 on ITO-coated glass (T3). All oxide surfaces were treated with OTS SAMs as described above and n^{++}-Si and ITO acted as gate electrodes, respectively. All three types of transistors were top-contact devices [as shown in Figure 3.3(a) for T1 and T2, and Figure 3.3(b) for T3].

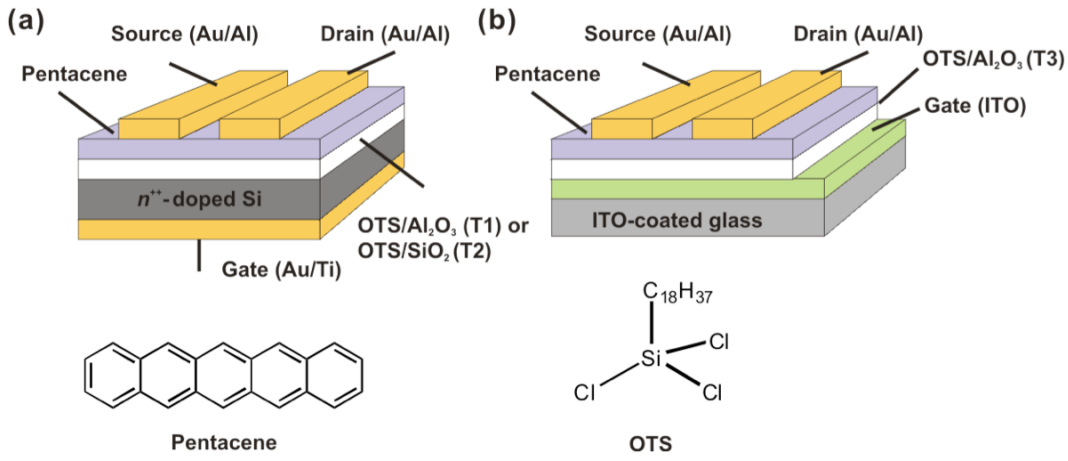


Figure 3.3: Diagram of the OFET device geometries for pentacene transistors (a) T1, T2 and (b) T3.

The transistors were fabricated by evaporating a 60 nm-thick film of pentacene on different substrates (T1, T2, and T3) followed by the patterned deposition of a 40 nm-thick Au film capped with a 100 nm-thick Al film to serve as top source/drain electrodes through a shadow mask. Here, a thin Au film was inserted to form a quasi-ohmic contact between pentacene and the source/drain electrodes. Ti/Au (10 nm/100 nm) backside metallization was used as the external gate contact in T1 and T2. Prior to deposition,

pentacene (Aldrich) was purified using gradient zone sublimation, and then deposited at a rate of 0.3 Å/s, as measured by a crystal monitor. The temperature and pressure during deposition were 25 °C and 2×10^{-8} Torr, respectively. The samples were transferred in a vacuum tight vessel without being exposed to atmospheric conditions into a N_2-filled glovebox (O_2, H_2O < 1 ppm) for electrical testing. The electrical measurements were performed using an Agilent E5272A source/monitor unit in a dark environment.

The surface morphology of the pentacene films on different substrates (T1, T2, and T3) was characterized using AFM as shown in Figure 3.2. The growth of pentacene films on all three OTS-treated substrates exhibited high structural order and displayed island formation, but no dendrite-like crystal formation was observed. However, the grain size varied greatly from the substrates with different surface energy and surface roughness. Therefore, although the *rms* roughness on T1 and T2 are comparable, the grain size was slightly reduced on T1 where its aqueous contact angle is lower. A further reduction in grain size can be seen in T3 due to its larger roughness (12 Å) compared to T1 and T2 [121, 122]. The larger grain size of pentacene films on T2 may be due to the residual polar groups on SiO_2, like OH^- and silanols [64].

Intermolecular layer spacing of pentacene films was determined by X-ray diffraction (XRD). As shown in Figure 3.2, the diffraction spectrum of island films consisted of crystalline peaks with a first diffraction peak at $2\Theta = 5.74$ º, corresponding to “thin film” spacing of 15.4 Å, and the presence of higher order peaks (up to 4 or 5) was observed on the smooth substrates (T1, T2). The lattice spacing corresponds to a tilt of the molecules of 17.1º to the surface normal, assuming a triclinic single crystal structure. The presence of a “bulk” phase of pentacene with a spacing of 14.4 Å was not

observed for films reported here. Peak intensity and the number of higher-order reflections mirrored the grain size of the crystalline structure observed in AFM images: films with larger grains showed higher intensity and more higher-order reflections. With smaller crystalline grain size, the peak intensity of T1 was slightly lower than that for T2. In comparison, the grain size was reduced and the peak intensity was decreased in T3 due to its large substrate surface roughness, as discussed by Steudel [121] and Fritz [122].

Pentacene transistors were characterized in the saturation regime defined by standard MOSFET models. To explore the influence of the different dielectrics (Al_2O_3 and SiO_2) on device performance, transistors T1 and T2 with a channel length $L = 65 \pm 5$ μm and a channel width $W = 590 \pm 90$ μm were compared. These two types of transistors had similar properties such as substrate surface roughness, pentacene morphology, and structural ordering as discussed earlier. Figure 3.4(a) shows the output characteristics (drain-source current I_{DS} vs. drain-source voltage V_{DS} for increasing values of gate-source voltage V_{GS}) and transfer characteristics ($|I_{DS}|$ vs. V_{GS} plotted on a logarithmic scale and $\sqrt{|I_{DS}|}$ vs. V_{GS}, at V_{DS} = -30 V) for the two transistors. Field-effect mobilities and threshold voltages were calculated in the saturation regime by fitting the $\sqrt{|I_{DS}|}$ vs. V_{GS} data to the square law [see Equation (3) and (6)].

A field-effect mobility of 1.5 ± 0.2 cm^2/Vs was extracted for the T1 transistors while the T2 transistors had a lower carrier mobility of 0.6 ± 0.1 cm^2/Vs. With Al_2O_3 (κ = 7.5) as a gate insulator, the capacitance density of the gate insulator in the T1 transistors was as high as 32.7 nF/cm^2 as compared to 17.3 nF/cm^2 in the T2 transistors. Consequently, the saturation current (-88 μA) in T1 transistors was almost 5 times larger than that (-17 μA) obtained from T2 transistors as shown in Figure 3.4(a).

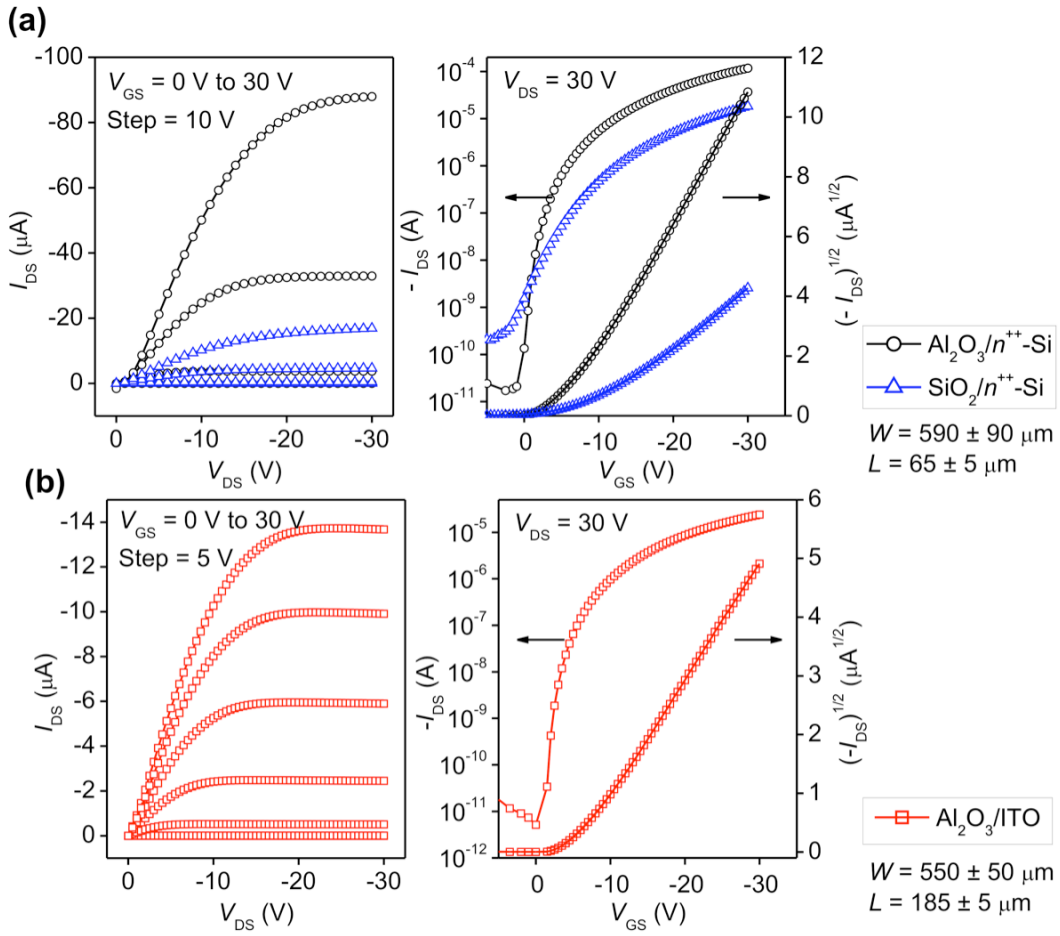


Figure 3.4: Transfer and output characteristics of *p*-channel pentacene OFETs (a) T1, T2 and (b) T3.

The higher mobility and current obtained from T1 transistors can be correlated to the morphology of the pentacene film and the dielectric/surface properties of OTS-treated Al_2O_3: first, compared with pentacene films on T2 (OTS-treated SiO_2), the reduced grains and a well-ordered island formation of pentacene films on OTS-treated Al_2O_3 (T1) indicate a higher interconnection and tighter packing (with improved contact) between grains, which could lead to more efficient charge transport and enhance the drain current in the channel [123]. Secondly, with OTS SAMs on the surface, the surface disorder

induced by the polar groups from high-κ dielectric surface (Al_2O_3 in our case) can be minimized. This is confirmed by the zero turn-on voltage (V_{TO}) shown on the transfer curve in Figure 3.4(a), indicating that no net fixed charges exist at the semiconductor/insulator interface. By using gate insulators with higher dielectric constant, a higher concentration of the charge carriers is accumulated in the channel for the same gate voltage and the Fermi level moves toward the band edge. The trapping states located in the 'gap' are filled and consequently a higher density of injected carriers is free to move with the microscopic mobility associated with carriers in the delocalized states. Thus, the use of high-κ dielectrics not only lowers the operating voltage, but also improves the mobility. This increase in mobility can be superlinear, as observed in this study, since it is due to the cumulative process of carriers becoming available at higher energies as the lower energy traps are filled. Using dielectric films with comparable thickness but having different dielectric constants, Dimitrakopolous *et al.* have demonstrated that the mechanism responsible for enhancing TFT carrier mobility is related to the carrier density in the channel region rather than the gate electric field [124].

Along with a zero turn-on voltage $V_{TO,}$ a low threshold voltage of -7 ± 2 V and a subthreshold slope of 0.6 V/decade were extracted for T1. A high on/off current ratio of 6×10^6 was also obtained for T1, measured between the "on" current value at V_{GS} = -30 V and the "off" current at V_{GS} = 0 V, both with V_{DS} = -30V. On the other hand, T2 showed a positive turn-on voltage V_{TO} of 5 V with a threshold voltage of -9 ± 2 V. Thus, the transistors were operated in the depletion mode instead of the enhancement mode as in T1, and consequently they could only be switched off by applying a positive gate bias**.** In addition, a higher subthreshold swing of 3 V/decade and a lower on/off ratio of 10^5 were

obtained for T2. The "off" current in T2 was 10 times higher than that in T1. These significant improvements in subthreshold slope, turn-on voltage (threshold voltage) and "off" current seen in T1 transistors can be attributed to a lower charge trap density at the pentacene/dielectric interface. We can estimate the maximum interfacial trap density $N_{trap}^{\max}$ from Equation (14) [125-127]:

$$N_{trap}^{\max} = \frac{C_{ox}}{q}\left[\frac{qS\log e}{k_B} - 1\right] \quad \textbf{(14)}$$

where k_B is Boltzmann's constant, T is temperature, q is the electronic charge, e is the base of the natural logarithm, C_{OX} is the capacitance density of the gate insulator, and S is the subthreshold slope in V/decade. Calculated from Equation (14), the trap density at the OTS-treated Al_2O_3 (T1) surface was as low as 1.8×10^{12} cm^{-2}, while a much higher value of trap density (5.2×10^{12} cm^{-2}) was obtained from the OTS-treated SiO_2 (T2) surface. According to these calculations, the number of residual OH groups is higher on OTS-treated SiO_2 than on OTS-treated Al_2O_3. However, this calculated trap density value for OTS-treated SiO_2 is comparable to previously reported values for bare SiO_2 [23], which could suggest a limited coverage of OTS on SiO_2. It has been shown that silanol groups on SiO_2 cannot be completely passivated by self-assembled alkyl layers [128]. This higher value can explain the positive turn-on voltage, larger subthreshold slope, and higher "off" current observed in T2. The interfacial traps are usually due to surface imperfections such as oxygen (OH groups), water molecules, or mobile ions. The residual silanol groups can trap electrons with protons and release H_2, therefore forming negative charges and inducing a positive shift in V_{TO} [64]. The electrical parameters we discussed here for transistors T1 and T2 along with those of the transistors T3 to be discussed next are summarized in Table 2.

Table 2: Summary of the electrical parameters for *p*-channel pentacene transistors T1, T2, and T3.

Pentacene OFETs	*rms* (Å)	Θ (°)	C_{OX} (nF/cm^2)	μ (cm^2/Vs)	V_T (V)	V_{TO} (V)	S (V/dec)	$I_{on/off}$ ×10^6
T1: OTS/Al_2O_3/n^{++}-Si	4.3	91	32.7	1.5 ± 0.2	-7 ± 2	0	0.6	6
T2: OTS/SiO_2/n^{++}-Si	4.0	112	17.3	0.6 ± 0.1	-9 ± 2	5	3	0.1
T3:OTS/Al_2O_3/ITO	12	92	32.7	0.9 ± 0.1	-6 ± 1	0	0.5	1

rms: root-mean-square roughness, Θ: contact angle, C_{OX} : capacitance density, μ: carrier mobility, V_T: threshold voltage, V_{TO}: turn-on voltage, S: subthreshold slope, $I_{on/off}$: on/off current ratio.

The output characteristics and transfer characteristics of T3 transistors are shown in Figure 3.4(b). Even though the substrate ITO-coated glass subtrates had a relatively large surface roughness [see Figure 3.2], a high field-effect mobility of 0.9 ± 0.1 cm^2/Vs was obtained in the saturation region for T3 with a channel length L = 185 ± 5 μm and a channel width W = 550 ± 50 μm. This value of mobility ranks to date as the highest known mobility reported for pentacene-based OFETs on ITO-coated glass [129]. This indicates that the contribution of higher carrier density to the field-effect mobility is dominant compared to the adverse effect of the substrate roughness on the morphology and transport. In addition to the high mobility values, T3 transistors exhibited superior electrical characteristics similar to those of T1: a turn-on voltage V_{TO} of zero volts, a threshold voltage of -6 ± 1 V, and a subthreshold slope of 0.5 V/decade, as shown on the transfer characteristic curve. The maximum trap density was estimated to be 1.4 × 10^{12} cm^{-2}, which is again close to the value estimated for T1. The consistency of trap density across the same type of oxide surface further confirms that Al_2O_3 has less trapping sites. A high on/off current ratio larger than 10^6 was also obtained from T3. Since pentacene growth, and thus pentacene-based OFETs, can be affected by the roughness of dielectric

layers underneath as demonstrated by Fritz [122], the high performance of T3 transistors demonstrates the effectiveness of employing an Al_2O_3 layer grown by ALD technique as a dielectric for inherently rough substrates.

3.1.3 Conclusions

In summary, we have utilized atomic layer deposition (ALD) to grow Al_2O_3 gate dielectric insulators and obtained high performance pentacene OFETs. OFETs fabricated on n^{++}-Si wafers and ITO-coated glass were operated in enhancement mode with a zero turn-on voltage, and exhibited large carrier mobility and a low threshold voltage, as well as a low subthreshold swing and a large on/off current ratio. Atomic force microscopy (AFM) images of pentacene films on Al_2O_3 revealed well-ordered island formation, and X-ray diffraction patterns showed characteristics of a “thin film” phase. Low trap density and high capacitance density of Al_2O_3 gate insulators also contributed to the high performance of pentacene field-effect transistors. The results of this work not only demonstrate that gate dielectrics grown by ALD present a viable alternative to dielectrics from traditional deposition techniques, but also show that the ALD dielectrics can result in improved electrical performance of transistors even on substrates with high roughness. The latter will become an increasingly critical issue in the future for most flexible substrates of interest.

3.2 Dielectric Interface Engineering with Polymeric Buffering Layers: Performance and Stability

The operational instability of OFETs, including hysteresis, reproducibility and reliability, and bias stress (BS) effect, is a remaining problem to be solved for practical

applications such as flexible displays and low cost RFIDs. The electrical instability induced by the BS effect is represented by both a drain-source current decay and a threshold voltage shift with prolonged operation time under a fixed gate voltage. There exist several potential mechanisms for the electrical instability, which include trapping of charges, defect generation [130], charge tunneling within the gate dielectrics, at the semiconductor/dielectric interface [131, 132], in the semiconductor itself, or at the interface near the source/drain contacts [133, 134]. The current instability has been investigated with different gate dielectric surfaces and the results indicate the SiOH groups and water molecules absorbed on the surface are the origins of the trap sites [135]. Low-κ polymeric dielectrics have been demonstrated as good dielectric insulators for organic transistors. The device performance of organic transistors was correlated with the dielectric surface energy and the glass transition temperature of polymers [64, 123, 136]. However, no polymeric interface providing both high electrical performance and good operational stability for *p*-channel OFETs has yet been identified.

This work was focused on the structural ordering, the electrical performance, and the operational stability of pentacene OFETs with hydroxyl-free low-κ polymers at the gate dielectric surfaces. The polymers chosen for this work are divinyltetramethyldisiloxane-bis(benzocyclobutene) (BCB) (Cyclotene^{TM}, Dow Chemicals) and polystyrene (PS) with their chemical structures drawn in Figure 3.5. Crosslinkable BCB can provide a high-quality hydroxyl-free interface [63] to the organic semiconductor with a high dielectric breakdown strength exceeding 3 MV/cm [137]. With poly (α-methylstyrene) (PMS) as a surface modification layer on gate dielectrics, 3M company obtained a record mobility as high as 7 cm^2 /V s with thin film pentacene

transistors [19]. Here, PS instead of PMS was used because PS lacks dipole moments (such as CH_3- in PMS).

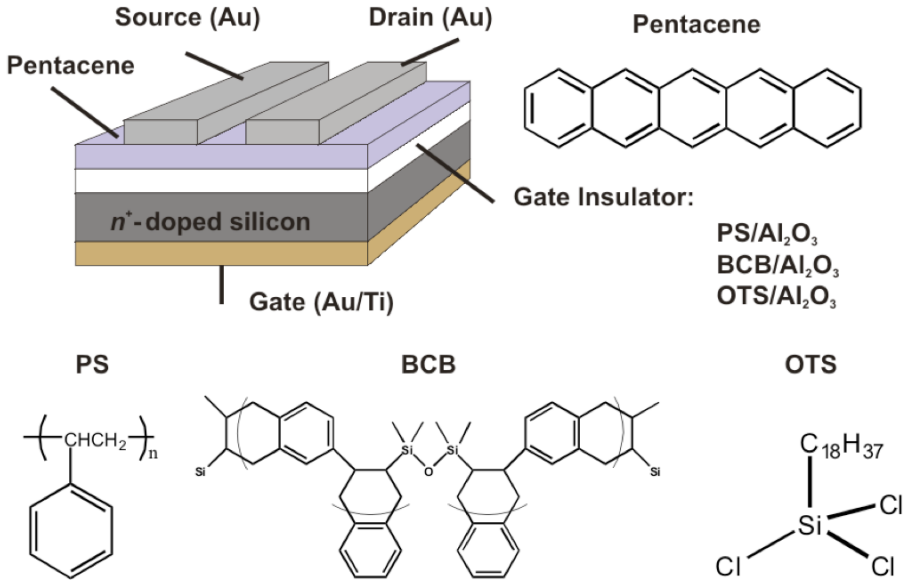


Figure 3.5: Schematic of a pentacene OFET along with the chemical structures of the materials used in the study.

3.2.1 Experimental Details

Pentacene transistors were fabricated on heavily n-doped silicon substrates (n^{++}-Si, as the gate electrode) with a 100 nm-thick Al_2O_3 layer deposited by atomic layer deposition (ALD) as a gate dielectric insulator. Top-contact OFET device geometry was used as shown in Figure 3.5. To better control the interfacial properties at the dielectric and the pentacene layer, as well as enhance the device operation stability and reproducibility, the Al_2O_3 dielectric surface was passivated with different hydroxyl-free

polymers (PS and BCB in this work) as thin buffer layers. The thin polymeric layers were formed and processed as follows. The BCB thin films from diluted Cyclotene^{TM} were crosslinked at 250 ºC on a hot plate for 1 hour in a N_2-filled glovebox. PS films were spin-coated from a 4 mg/ml solution in toluene and annealed at 130 ºC on a hot plate for 1 hour. The Al_2O_3 surface was also modified with OTS SAM molecules. OTS has been widely known as a good tunnel barrier to hydroxyl groups on oxide surfaces due to its long alkyl chain, and a good surface layer for controlling structural order of pentacene films. The OTS layer was formed by soaking the substrates in a 5 mM toluene solution of OTS for 15 hours in a dry N_2-filled glovebox.

The capacitance density C_{OX} (nF/cm^2) was measured from parallel-plate capacitors with 12 varying contact areas. The added buffer layer on Al_2O_3 reduced the capacitance density $C_{OX,}$ from 66.4 nF/cm^2 to 64.1 nF/cm^2 with OTS, 46.8 nF/cm^2 with BCB, and 42.7 nF/cm^2 with PS, respectively. The results on C_{OX} are listed in Table 3 and were used to calculate the OFET electrical parameters.

Table 3: Summary of the electrical parameters for *p*-channel pentacene OFETs with different dielectric surfaces.

	rms **(Å)**	***Θ*** **(°)**	C_{OX} **(nF/cm^2)**	***μ*** **(cm^2/Vs)**	V_{TO}**/** V_T **(V/V)**	***S*** **(V/dec)**	$I_{on/off}$ **×10^5**	***τ*** **(s)**	***β***
PS/Al_2O_3	2.3	84	42.7	0.64	-1.6/-3.39	0.20	7.2	1.5×10^8	0.41
BCB/ Al_2O_3	2.4	86	46.8	0.47	-1.6/-3.62	0.26	3.8	2.4×10^5	0.41
OTS/ Al_2O_3	4.1	98	64.1	0.36	0.2/-0.86	0.30	1.7	2.1×10^6	0.42

rms: root-mean-square surface roughness, *Θ*:water contact angle on the dielectric surface, *μ*: field-effect mobility, V_{TO}: turn-on voltage, V_T: threshold voltage, *S*: subthreshold slope, $I_{on/off}$: on/off current ratio, *τ*: characteristic trapping time, and *β*: dispersion parameters.

Pentacene (Aldrich), purified using gradient zone sublimation, was deposited at a rate of 1 Å/s to a thickness of 50 nm. 60 nm-thick Au as S/D electrodes was deposited at a rate 1 Å/s on top of the pentacene through a shadow mask in the same chamber without breaking the vacuum. The substrates were held unheated during the deposition and the chamber vacuum was about 5×10^{-8} Torr. The samples were transferred in a vacuum tight vessel without being exposed to atmospheric conditions into a N_2-filled glovebox (O_2, H_2O < 1 ppm) for electrical testing. The electrical measurements were performed using an Agilent E5272A source/monitor unit under dark conditions.

To characterize the surface properties, the surface morphology of Al_2O_3 with different surface modification layers was investigated by AFM. The root-mean-square (*rms*) surface roughness of the dielectric surfaces with different surface treatment was estimated to be below 5 Å when measured over an area of 1 μm × 1 μm, as listed in Table 3. With polymeric surfaces, the dielectric surface roughness of the Al_2O_3 film was even further smoothed to be less than 3 Å during spin coating. The effect of surface roughness on the charge transport at the interface can be negligible for an *rms* value smaller than 5 Å [121, 122]. The surface energy of the dielectric surface with different buffering layers was studied by contact angle measurement using DI water, with the results listed in Table 3. All the surfaces became highly hydrophobic with aqueous contact angles around 90 degrees, indicating low surface energy with BCB, PS, or OTS on the dielectric surface.

The morphology of pentacene films can be affected by the deposition conditions (substrate temperature, deposition rate, and thickness) as well as the dielectric surface properties (surface roughness, surface energy, etc.). With the same deposition conditions for pentacene, this work investigated the effect of dielectric properties on the structural

ordering of pentacene films and correlated them with the device performance. Here, AFM and x-ray diffraction (XRD) were used to characterize the film morphology and the structural ordering of pentacene molecules, as illustrated in Figure 3.6.

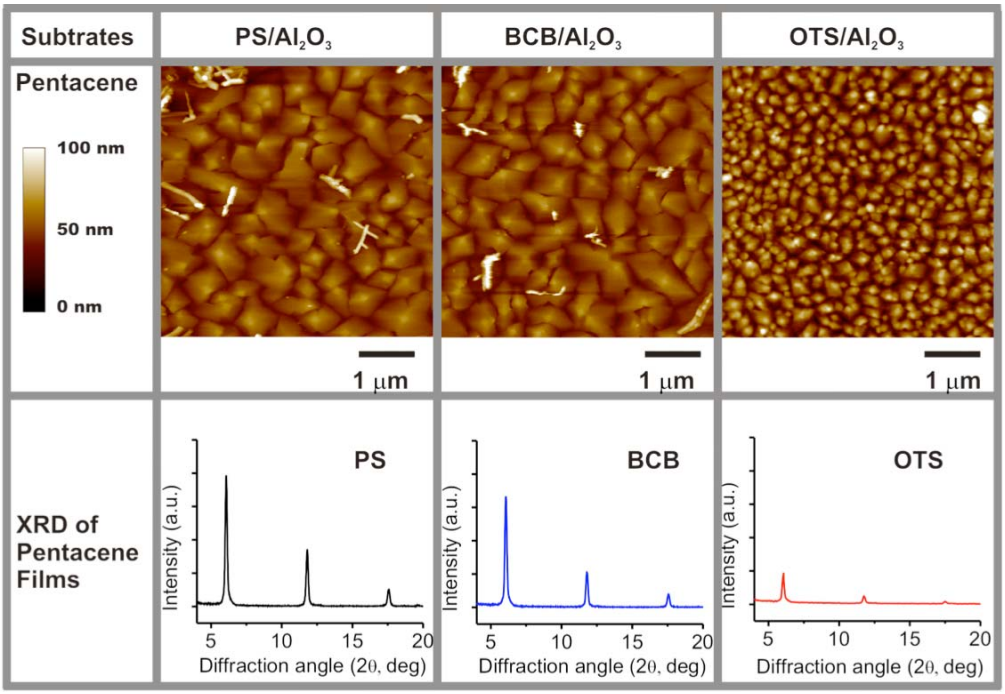


Figure 3.6: AFM images and XRD patterns of pentacene films on the different dielectric surfaces.

Pentacene films on all dielectric surfaces exhibited high structural order and displayed island formation. However, the grain size varied greatly for the substrates with different surface energy and surface roughness. The morphology of pentacene shows small grains on OTS-treated Al_2O_3, probably caused by the large surface roughness of the dielectric. The pentacene growth on the smoother dielectric surfaces (PS and BCB), on the other hand, was less disturbed and prone to form large grains with good connectivity.

The slight difference of the grain size with PS and BCB can be attributed to the different surface energy. The diffraction spectrum of island films consisted of crystalline peaks with a first diffraction peak at $2\Theta = 5.74$ º, corresponding to "thin film" spacing of 15.4 Å; the presence of a "bulk" phase of pentacene with a spacing of 14.4 Å was not observed since the substrate temperature was held at room temperature during deposition. The XRD peak intensity mirrored the grain size of the crystalline structure observed in the AFM images: Films with larger grains showed higher intensity.

3.2.2 Operational Stability and Electrical Characterization

In order to accurately characterize the device performance, the devices need to stay stable during measurement. Testing procedures like hysteretic scans and duty-cycle tests were used to test the stability and reproducibility of the devices. The fabrication and testing were carried out in a N_2-filled glove box under dark conditions so that device instability induced by light, water, and oxygen was avoided. The electrical instability/degradation is attributed to trapping at both the shallow states and deep states. For deeper trapping sites, longer trapping time/relaxation time is required. The trapping at the shallow sites is usually reversible even at room temperature. The ratio and distribution of shallow and deep traps are dependent on the materials, fabrication, and device operation. Electrical instability induced by the trapping on the different time scales can manifest as hysteresis, current decay, or threshold voltage shift. The devices showing hysteresis are least stable, and this property is highly undesirable when not used as memory devices.

The hysteretic transfer characteristics were measured with a resolution of 20 ms and duration of several seconds in the saturation regime with V_{DS} = -10 V. The

representative transfer curves and normalized output curves (I_{DS} was normalized by the capacitance density C_{OX}) are compared in Figure 3.7 for the devices with the same geometry (channel length L of 100 μm and channel width W of 1000 μm) and different dielectric surface treatments. On the time scale of this measurement, negligible hysteresis and threshold voltage shift were found in transistors with either polymeric dielectric surface or OTS-treated dielectric surface.

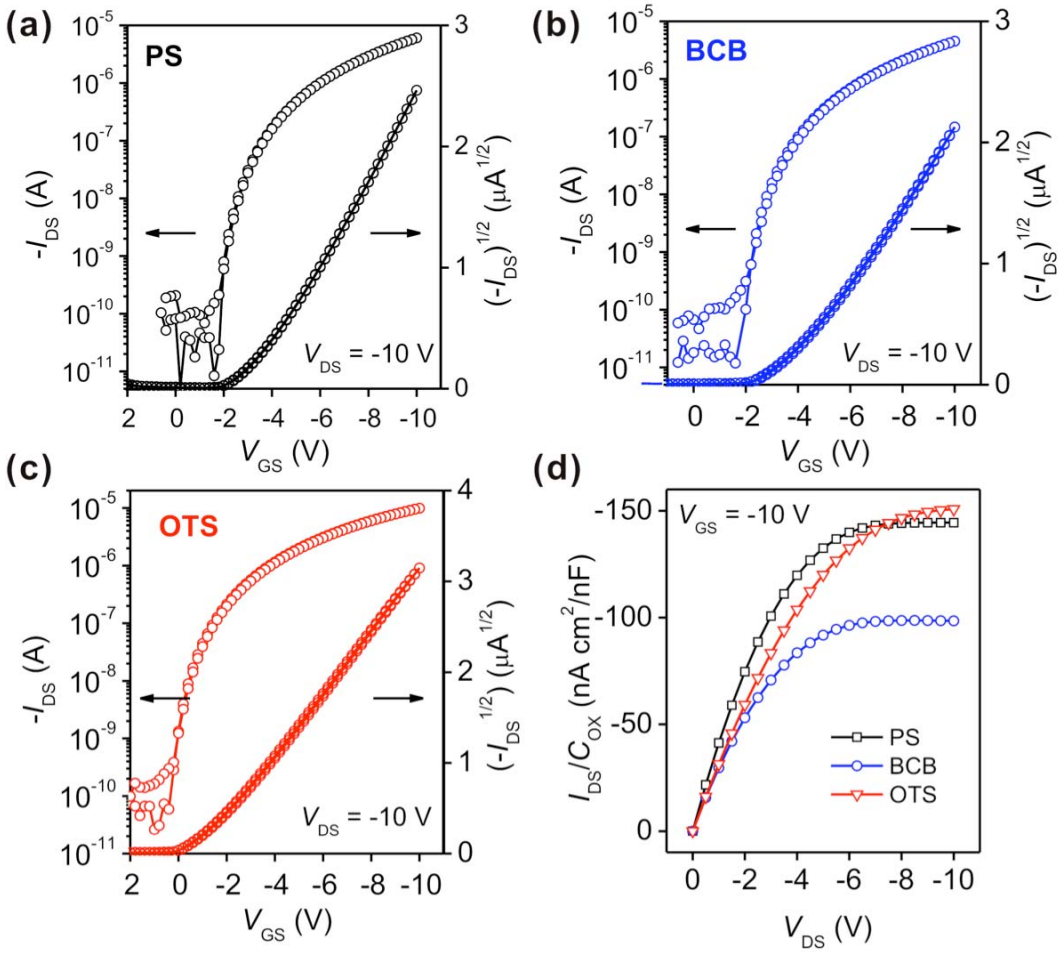


Figure 3.7: (a) to (c) hysteretic transfer characteristics with V_{DS} = -10 V. (d) Comparison of output characteristics (normalized with C_{OX}) with V_{GS} = -10 V.

Next, all the devices were repeatedly stressed by measuring transfer characteristics in the saturation regime 100 times with a 2s waiting time between cycles. The measured transfer curves from the first 10 cycles and the last 10 cycles were superimposed and are shown in Figure 3.8. Again, no significant performance degradation was observed in any transistors including the ones with OTS SAM. The shape of the successive transfer curves remained unchanged during hysteretic scans and during 100 duty-cycle scans, indicating that there exist no shallow states from structure defects within the semiconductor or the gate dielectric caused by the applied gate field [138].

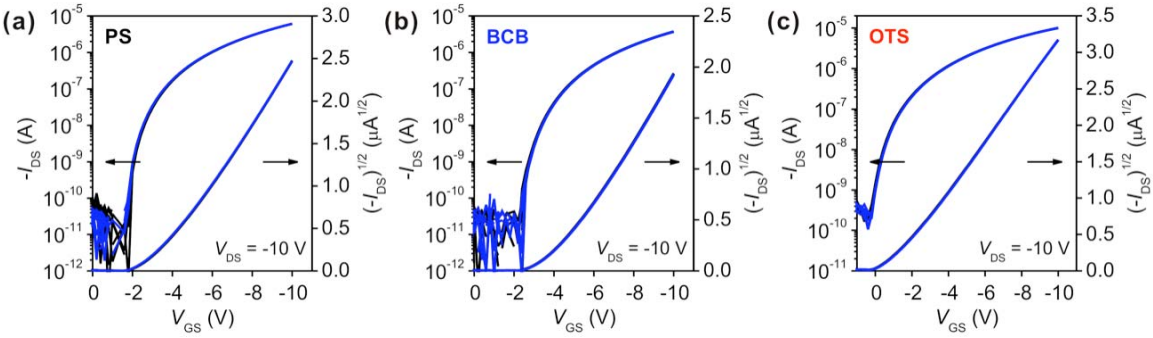


Figure 3.8: Superimposed transfer curves from the first 10 scans (black) and the last scans (blue) during a duty-cycle-like test with 100 scans and 2s rest time between cycles for pentacene transistors with different dielectric interfaces: (a) PS, (b) BCB, and (c) OTS.

In these two types of measurements, the rest time between stressing is from 20 ms to several seconds. We can speculate that either no fast trapping occurred or the trapped charges were detrapped/released during the rest time. Negligible threshold voltage shift occurred at this time-scale, showing a good electrical stability and reproducibility for

devices under normal operation using Al_2O_3 gate dielectrics with PS, BCB, and OTS surfaces. This is attributed to the low concentration of shallows traps on the dielectric surfaces since the trapping species on Al_2O_3 surfaces, such as highly polar $Al(OH)_3$, absorbed water molecules and other impurities, and were screened by hydroxyl-free polymers or OTS SAM molecules.

With good stability under normal operating conditions, the device performance parameters can be extracted reliably from a forward gate bias scan as seen in Figure 3.7. Field-effect mobilities μ and threshold voltages V_T were calculated in the saturation regime defined by standard MOSFET models by fitting the $\sqrt{|I_{DS}|}$ vs. V_{GS} data to the square law. Also extracted from the transfer characteristics are the turn-on voltage (V_{TO}) and the on/off current ratio ($I_{on/off}$). The extracted electrical parameters (μ, V_{TO}, V_T, S, and $I_{on/off}$) are summarized and compared in Table 3 along with *rms* values and C_{OX} previously measured.

Devices with PS and BCB dielectric surfaces show similar electrical performance with high mobility, low subthreshold slopes, and high on/off current ratios. The higher mobility from pentacene transistors on PS can be correlated to the structural ordering of pentacene films: larger grains, higher XRD intensity and less trapping. Since OTS can not fully passivate the $Al(OH)_3$ groups on the surface, these electron-trapping residuals can act as dopants for hole transport, which gives rise to an earlier turn-on voltage and lower threshold voltages in pentacene OFETs with OTS.

To investigate the dependence of mobility on the channel length L, field-effect mobilities of devices are statistically plotted over the inverse of channel length (L^{-1}) with a channel width W = 1000 μm in Figure 3.9(a). All the devices with different dielectric

surfaces show a similar trend: the mobility remains nearly independent of channel length until reduced to 25 μm. The device mobility with short channels of 25 μm increases instead of decreasing like in many organic transistors where the channel current is contact-limited due to the large Schottky barrier at the metal/organic interface. The higher mobilities of short-channel devices could be explained as fewer traps from the grain boundaries present within a shorter range. It also implies a very low contact resistance and good ohmic contact between Au S/D electrode and pentacene films.

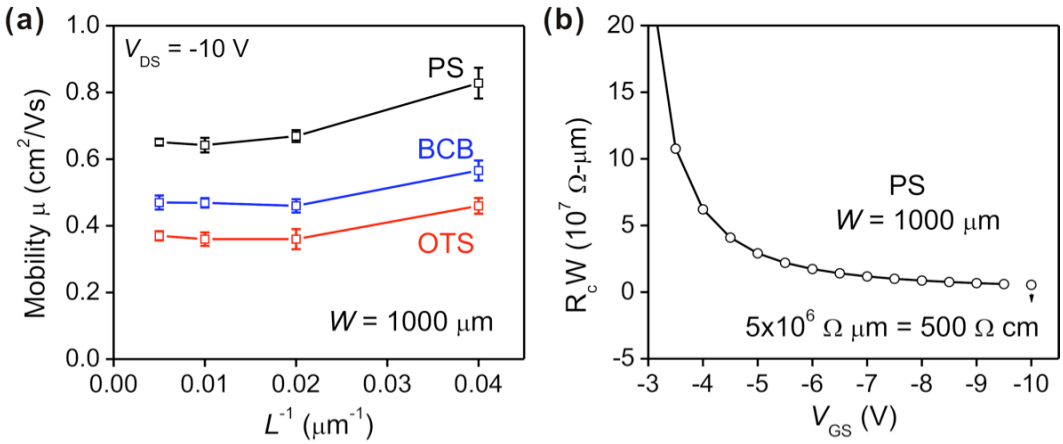


Figure 3.9: (a) The dependence of mobility on the inverse of channel length. (b) The width-normalized contact resistance obtained from pentacene OFETs with PS dielectric interface.

To gain a better understanding of the contact effect on the mobility, the contact resistance of pentacene transistors with PS as a surface treatment layer was extracted using a transmission line method (TLM) based on the dependence of current-voltage characteristics on channel length. In the linear regime, the overall device resistance R_{on} can be considered as the sum of the channel resistance R_{ch} and a total contact resistance

R_C according to Rolland [99]. A set of devices with channel lengths ranging from L = 50 μm to 200 μm and a fixed channel width of W = 1000 μm was used to calculate the contact resistance at a low drain-source voltage (V_{DS}) of - 0.1 V for V_{GS} values ranging from -3 V to -10 V. The width-normalized contact resistance ($R_C W$) was estimated using the y intercept of the least squares when extrapolating $R_{on}W$ to L = 0 μm, as plotted in Figure 3.9(b). The contact resistance drops drastically with V_{GS} since the resistance of the pentacene film was reduced by the increasingly induced charge density in the accumulation regime with V_{GS}. A low $R_C W$ of 500 Ωcm was achieved at V_{GS} = -10 V. This value is even lower than the best result reported by Klauk [139]. Since the contact resistance between the Au S/D electrodes and pentacene films is quite low and the values are similar for the devices with different dielectric surfaces, its change during the operation can be negligible compared to that of the channel resistance with a long channel length such as L = 100 μm. Therefore, the effect of contact resistance on the electrical stability can be justifiably ignored in this study.

3.2.3 Bias Stress Effect

To further explore the effect of different dielectric interfaces on the stability of pentacene transistors, the time-dependent decay of I_{DS} was tested under dc bias stress with V_{GS} = V_{DS} = -10 V for 1 hour, as plotted in Figure 3.10(a). The current decay in this experiment exhibited typical features of bias stress instability showing an exponential decay function. The trapping rate slows down with stressing time since the density of the vacant trapping sites decreases as more holes are trapped with time. Then these trapped charges screen the electrical field and in turn cause the negative shift of the threshold voltage.

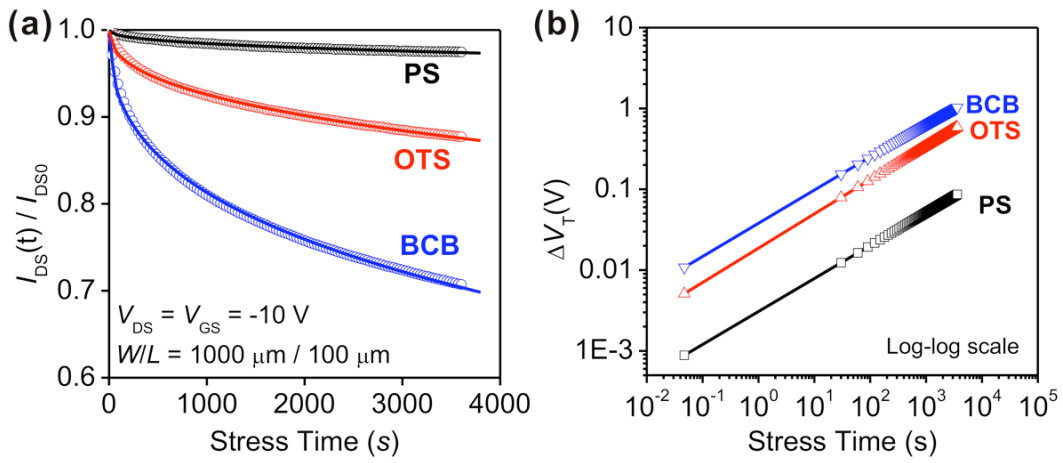


Figure 3.10: (a) Channel current decay when stressed with V_{GS} = V_{DS} = -10 V for 1 hour with a resolution of 20 ms. The points are experimental data and the dash lines are the fitting curves using Equation (19). (b) Threshold voltage shift ΔV_T was simulated with the fitting parameters obtained from Figure 3.10(a).

The bias stress instability can be described by a stretched exponential function based on threshold voltage shift (ΔV_T) or drain-source channel current decay. A stretched-exponential equation was proposed by Libsch and Kanicki [140] based on ΔV_T:

$$|\Delta V_T(t)| = |V_{GS} - V_{T0}|\{1 - \exp[-(\frac{t}{\tau})^{\beta}]\} \quad \textbf{(15)}$$

$V_{GS} - V_{T0}$ is the effective voltage drop across the gate insulator and V_{T0} is the initial threshold voltage at t = 0 s. The dispersion parameter β reflects the width of the involved trap distribution, and $\tau = \tau_o \exp(\frac{E_\tau}{kT})$ represents the characteristic trapping time of the carriers. In the model, the thermal activation energy E_a is given by $E_a = E_\tau \beta$, where β is the stretched exponential factor. $E_\tau = E_a / \beta$ is interpreted as the average effective energy barrier that carriers in the channel need to overcome before they can enter the insulator.

The above model can be extended with the measurement of drain-source channel on-current decay with time under dc bias stress [141]. Using on-current degradation instead of threshold voltage shift to estimate stability can avoid the error and inaccuracy caused by the measurement and extraction of the threshold voltage. The derivation of a stretched exponential function based on on-current degradation is described as follows.

The current-voltage characteristics in the saturation regime can be described as:

$$I_{DS} = \frac{1}{2}\mu C_{OX}\frac{W}{L}(V_{GS} - V_{T0})^2 = K(V_{GS} - V_{T0})^2 \quad \textbf{(16)}$$

When the device has been operated for a long period of time *t*, resulting in a threshold-voltage shift ΔV_T, the current-voltage characteristics at time *t* can be shown as:

$$I_{DS}(t) = K[V_{GS} - (V_{T0} + \Delta V_T(t)]^2 \quad \textbf{(17)}$$

Then the current decay with time $\Delta I_{DS}(t)$ can be described as:

$$\Delta I_{DS}(t) = \frac{I_{DS}(t)}{I_{DS0}} = \frac{[V_{GS} - (V_{T0} + \Delta V_T(t)]^2}{(V_{GS} - V_{T0})^2} \quad \textbf{(18)}$$

Combining the stretched-exponential function for ΔV_T from Equation (15), stretched-exponential function for $\Delta I_{DS}(t)$ can be reduced to:

$$\Delta I_{DS}(t) = \frac{I_{DS}(t)}{I_{DS0}} = \exp[-2(\frac{t}{\tau})^{\beta}] \quad \textbf{(19)}$$

As shown in Figure 3.10(a), the solid points are the experimental data and the dash line is the fitting data from Equation (19). The simulated results indicate that the experimental data are consistent with Equation (19) where the on current in the channel was obtained in the saturation regime.

The threshold voltage shift under the same condition can be calculated from Equation (15) using the fitting parameters extracted from Equation (19) (listed in Table 3), as shown in Figure 3.10(b). The dispersion parameter β, reflecting the width of the involved trap distribution, is very similar (0.41 to 0.42) in the devices with polymeric interfaces and SAM. The results are similar to the value obtained by Mathijssen [132, 142] using hexamethyldisilazane (HMDS) SAM to passivate the dielectric surface. The β value was found to be lower with higher HMDS coverage [132]. The stability during dc bias stress can be quantitatively compared with trapping time τ at room temperature. Longer τ implies higher stability, and less threshold voltage shift. Since polar $Al(OH)_3$ groups can act as traps, the presence of a spatial barrier between the mobile charge carriers and the traps results in a much longer time scale for the threshold voltage shift dynamics. Therefore, the stability of the devices with treated dielectric surfaces (PS, BCB or OTS SAM) was improved with long τ in the range of 10^5-10^8 s and with small ΔV_T below 1 V. Among them, pentacene OFETs with a PS-treated gate dielectric surface show the highest stability with the trapping time even longer than that of amorphous Si thin film transistors (TFTs) [143]. The extraordinary stability of PS dielectrics gives the pentacene transistors negligible ΔV_T of 0.2 V after 3600s stressed under dc bias with V_{GS} = V_{DS} = -10 V. Devices with OTS-treated surfaces also show good stability with time constants in the range of 10^6-10^7s, which agrees well with the results reported by Miyadera using β-phenethyltrichlorosilane SAM [144].

Surprisingly, stability with BCB-treated gate dielectrics in pentacene OFETs is poorer than PS as well as the OTS SAM surface in this work. This observation is distinctively different from *n*-channel C_{60} OFETs where BCB-treated gate dielectrics are

most stable [145]. In C_{60} *n*-channel transistors, the instability mostly results from the electron trapping from OH^- related groups on the dielectric surface. However, the bias stress induced instability in pentacene OFETs was not only from OH^- related groups but also from other mobile impurities at the interface or within the dielectrics. Crosslinked BCB and its monomers are all non-polar and the film was fully crosslinked in a dry environment. There were no intramolecular dipoles from the polymer or dipoles from the residual solvent. However, an additive (polymerized 1, 2-Dihydro-2, 2, 4-trimethylquinoline) was added in the BCB formulation as an antioxidant. These molecules remain in the polymeric dielectrics and at the surface after film processing. The molecules have lower molecular weight compared with the polymer, hence can act as true mobile dipoles. Once the negative terminal of the dipoles aggregates near a hole, this site becomes a trap for the holes [115]. When a negative electrical field is applied across the gate, the negative terminal of the dipoles moves toward the holes and immobilizes them. The displacement of dipoles on the insulator surface could reduce the current I_{DS} along the interface where the charge transport occurs. However, there are no experiemental data to verify this theory. Further investigation is required to explore the origin of slow trapping at the interface between BCB and pentacene.

The characteristic trapping time τ (10^5-10^8) is several orders of magnitude longer than the time duration for hysteresis and repeatability (10^{-3}-10s) testing. In other words, when the devices experience short-term stress, no bias stress effect is introduced. To further investigate the trap distribution and the activation energy of traps, the measurement of current decay at various temperatures is required.

This model is able to predict the threshold shift behavior in any time duration. However, this model only addresses the electrical stress with dc bias. In AMLCD, a-Si:H TFTs are subjected to pulsed gate-bias addressing with a typical frequency of 60 Hz [11]. The magnitude of threshold voltage shift caused by ac stress or pulsed gate bias is significantly lower. A logical explanation is that the trapped charges at the shallow states will be released if the rest time between the testing is longer than the trapped time.

3.2.4 Conclusions

The device performance and operational stability of pentacene OFETs were investigated based on PS and BCB polymeric dielectric interfaces and OTS-treated surface dielectrics. The device performance was correlated with the structural ordering of pentacene films and the surface properties of gate dielectrics. Both PS and BCB can provide high device mobility corresponding to the large grain size on the smooth surface with low surface energy. However, when measured under prolonged dc gate bias, the electrical performance of devices with BCB deteriorates even faster than the ones with OTS-treated dielectric surface. It is suspected that the impurities in the BCB formulation act as long-lived trapping sites. With PS at the gate dielectric surfaces, pentacene OFETs show good electrical performance, extraordinary electrical stability, and low contact resistance.

CHAPTER 4 N-CHANNEL C_{60} OFETS

Complementary organic-based circuits (utilizing both *n*-channel and *p*-channel transistors) are of great interest in organic electronics, driven by the demand for low-cost, large-area, flexible devices processed at low temperature and low power. To date, a major challenge has been to improve the discrete device performance of *n*-channel organic field-effect transistors (OFETs). Recently, Klauk [43] demonstrated ultralow-power consumption complementary circuits using monolayer gate dielectrics. However, as in many other reports of organic complementary circuits [42, 45], F_{16}CuPC *n*-channel OFETs showed inferior performance to their counterpart (pentacene *p*-channel OFETs) with a mobility more than one order of magnitude lower. On the other hand, electron mobilities as high as 4.9 cm^2/Vs and 6 cm^2/Vs have been reported by Itaka [26] and Anthopoulos [25] in C_{60} devices when operated at high voltage (> 60 V). In the former report, the on/off current ratio was reduced by the use of pentacene (a well-known *p*-type semiconductor) layer at the dielectric/semiconductor interface. In the latter report, C_{60} was deposited by hot wall epitaxy (HWE) requiring deposition temperatures as high as 250 ºC. Although low-voltage C_{60} OFETs were demonstrated with a triple layer gate insulator of SiO_2 /ZSO/SiO_2 and a low level of hysteresis [27], the threshold voltage of 1.9 V was high compared with the applied voltage of 5 V. Recently, we reported on high-mobility OFETs based on C_{60} processed at room temperature, but the performance was shown to degrade at short channel lengths [145].

Many reports on *n*-channel OFETs focus on the design and synthesis of novel *n*-type semiconductors to improve air-stability, solution processibility, and mobility

through tailoring of the chemical structures [29, 30, 33, 146]. However, the electrical characteristics of OFETs are governed not only by the properties of the semiconductor material but also by the boundary conditions imposed by the device architecture at the contacts and interfaces. For example, low electron mobilities measured in *n*-channel OFETs are often due to high contact resistance imposed by the injection barrier height between the *n*-type organic semiconductor and the source and drain electrodes. This high contact resistance can greatly limit the switching frequency of the *n*-channel OFETs due to a significant degradation of effective electron mobility upon channel scaling. However, the issue of contact resistance in *n*-channel OFETs, which is far more severe than that of *p*-channel OFETs, has not yet been widely studied. It has been established that for *p*-channel OFETs, the performance of devices is also governed by the dielectric surface properties at the insulator/semiconductor interface that often affect the structure of the semiconductor film [61, 62]. In the case of *n*-channel OFETs, electron trapping at the interface from carbonyl, hydroxyl, and silanol groups has been confirmed as a primary limiting factor for *n*-channel conduction and a major contribution to large threshold voltage [63, 64]. Hence, *n*-channel OFET performance is often limited by the essential electrode/semiconductor and dielectric/semiconductor interfaces rather than the properties of the semiconductors themselves.

In this work, the research on *n*-channel OFETs emphasizes the interface engineering both at the dielectric/semiconductor and at the electrode/semiconductor. Section 4.1 studies on the compatibility between the modified dielectric surface (with thin polymeric buffering layers) and *n*-channel semiconductor, C_{60} in this case. The electrical performance as well as the operational stability is characterized and compared.

The uniformity of device performance over the large area is going to be demonstrated with one of the polymers as an example. With an optimal dielectric surface, Section 4.2 presents the research work on the reduction of contact resistance between the source/drain electrodes and C_{60} using metal contacts with different work function. The effect of the channel length on the charge mobility is explored and correlated with the contact resistance extracted by a transmission line method. The motivation for this work is to eventually achieve high performance, low voltage *n*-channel OFETs with short channel and good operational stability, by combining high-κ gate dielectrics with trapping-free surface treatment and low work-function metals to reduce the source/drain contact resistance.

4.1 Polymeric Smoothing Layer as Surface Modification of Gate Dielectrics

4.1.1 Experimental Details

The study of dielectric surface modification with polymeric buffering layer was conducted based on *n*-channel C_{60} OFETs. Transistors were fabricated on heavily *n*-doped silicon substrates (n^{++}-Si, as the gate electrode) with 200 nm-thick thermally grown SiO_2 as the gate dielectric ($\kappa = 3.9$), as shown in Figure 4.1. To better control the interfacial properties at the dielectric and C_{60}, the SiO_2 dielectric surface was passivated with different thin buffer layers of polymers or with SAMs. Three hydroxyl-free polymers: BCB (Cyclotene^{TM}, Dow Chemicals), polystyrene (PS), and poly (methyl methacrylate) (PMMA) were used to coat the SiO_2 surface. The thin films from diluted Cyclotene^{TM} BCB were crosslinked at 250 ºC on a hot plate for 1 hour in a N_2-filled glovebox. PS or PMMA films were spin-coated from a 4 mg/ml solution in toluene and

annealed at 130 ºC on a hot plate for 1 hour. Octadecyltrichlorosilane (OTS) SAM with a long alkyl chain, known as a good tunnel barrier to silanol groups on SiO_2 surface, was formed by soaking the substrates in a 5 mM toluene solution of OTS for 15 hours in a dry N_2-filled glovebox, right after the substrates were oxygen-plasma treated for two minutes. The thickness of the OTS layer was 2.25 nm as measured by ellipsometry.

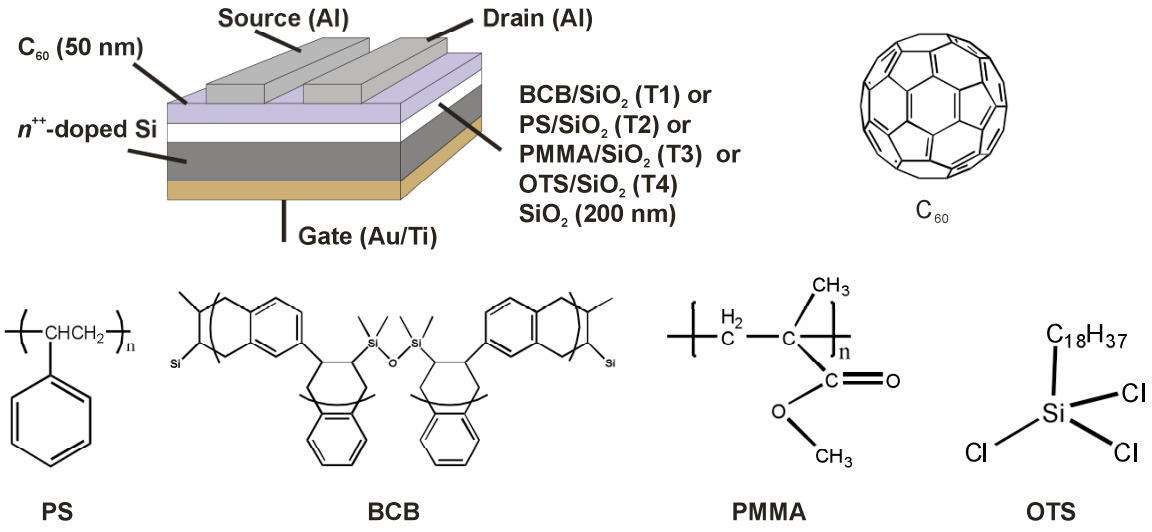


Figure 4.1: Diagram of the OFET device geometries for transistors T1 to T4.

The surface roughness (*rms*) of both polymer-coated and OTS-treated 200 nm-thick SiO_2 was below 5 Å as measured by AFM. However, their aqueous contact angles (Θ) are different where OTS-treated SiO_2 is the most hydrophobic (Θ = 98°) and PMMA-treated SiO_2 is the least hydrophobic (Θ = 66°). The AFM images and the contact angles of the substrates are displayed in Figure 4.2 along with the AFM images of C_{60} film grown on these substrates. The capacitance density C_{OX} (nF/cm^2) was measured from

parallel-plate capacitors with 12 varying contact areas. The buffer layer on SiO_2 reduced C_{OX} from 16.6 to 16.2 nF/cm^2 with OTS, 15.5 nF/cm^2 with BCB, 15.3 nF/cm^2 with PS, and 15.8 nF/cm^2 with PMMA, respectively. The results on *rms* and C_{OX} are listed in Table 4 and will be used in the calculation of OFET electrical parameters.

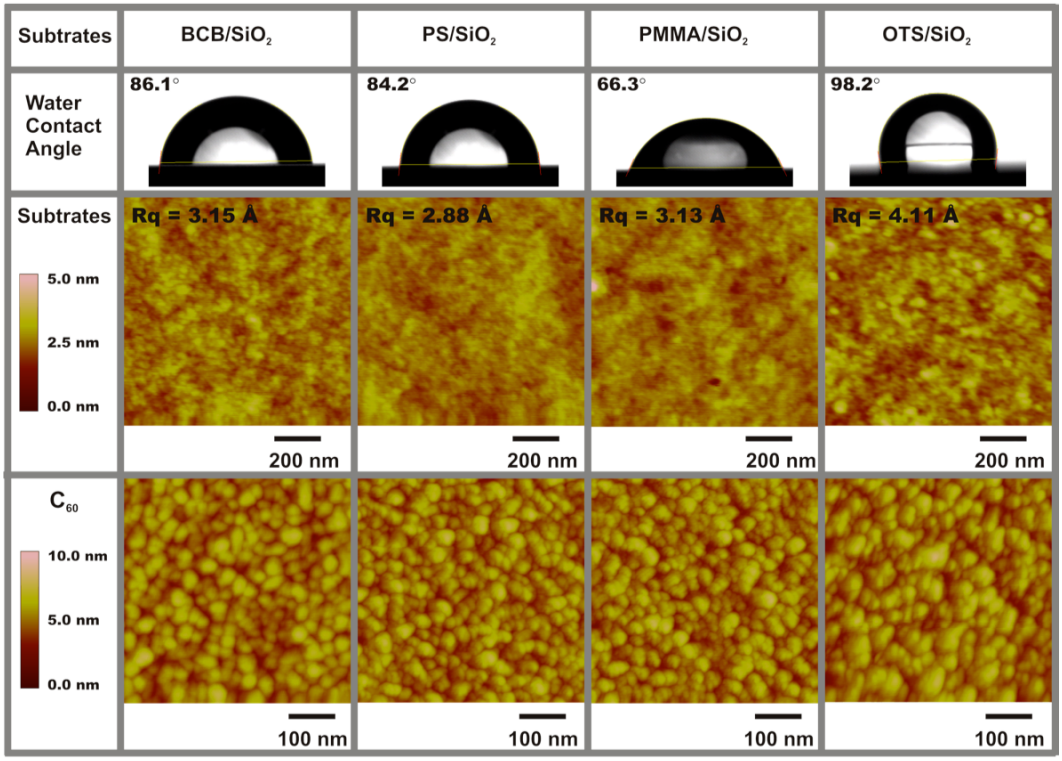


Figure 4.2: AFM images of C_{60} films grown on the different polymeric surfaces.

For convenience, the transistors with BCB, PS, PMMA, and OTS as a buffer layer are referred to as devices T1, T2, T3, and T4, respectively. All transistors, for which data are reported here, underwent the same processing, measurement, and analysis steps. The devices were completed by evaporating a 50 nm-thick film of purified C_{60} at room

temperature followed by the shadow mask deposition of the patterned 150 nm-thick Al as top source/drain electrodes. The electrical measurements were performed in a N_2-filled glovebox (O_2, H_2O < 0.1 ppm) at normal pressure (1 atmosphere) in the dark using an Agilent E5272A source/monitor unit.

4.1.2 Electrical Characterization

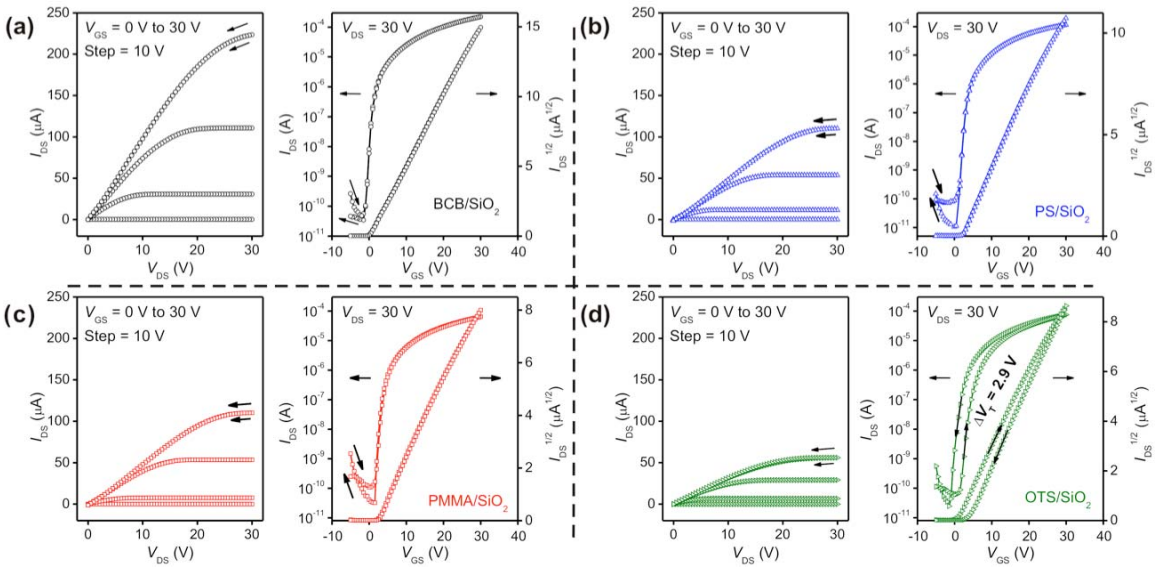


Figure 4.3: Output and transfer characteristics of both forward and reverse gate bias scan for C_{60} transistors T1 (a), T2 (b), T3 (c), and T4 (d).

To explore the influence of the different dielectrics on device performance, the representative output and hysteretic transfer electrical characteristics of transistors T1, T2, T3 and T4 with the same channel length L = 100 μm and the same channel width W = 1000 μm are compared in Figure 4.3. Field-effect mobilities μ and threshold voltages V_T

were calculated in the saturation regime defined by standard MOSFET models by fitting the $\sqrt{I_{DS}}$ vs. V_{GS} data to the square law. Also extracted from the transfer characteristics are the turn-on voltage (V_{TO}) and the on/off current ratio ($I_{on/off}$). For each type of transistor, four devices with identical geometry were measured to obtain the mean value with its standard derivation (SD). The extracted electrical parameters (μ, V_{TO}, V_T, S, and $I_{on/off}$) (calculated from forward bias scans) are summarized and compared in Table 4, along with *rms* and C_{OX} previously obtained.

As seen from AFM height images in Figure 4.2, C_{60} films generally exhibit similar morphology and microstructure with small grains, regardless of the dielectric surface modification. This structure exhibits similar characteristics as that observed previously in C_{60} films deposited at low temperature [22, 147]. Even with small grains in C_{60} films, all transistors presented a mobility μ higher than 1 cm^2/Vs, a threshold voltage V_T less than 2.5 V, a subthreshold slope S steeper than 1 V/decade, and $I_{on/off}$ ratios larger than 10^6. Note that among them, T1 (BCB) showed the highest mobility of 3.1 ± 0.2 cm^2/Vs.

Table 4: Summary of the electrical parameters for C_{60} transistors T1, T2, T3, and T4.

C_{60} OFETs	*rms* (Å)	Θ (°)	C_{OX} (nF/cm^2)	μ (cm^2/Vs)	V_{TO} (V)	V_T (V)	S (V/decade)	$I_{on/off}$ $\times 10^6$
T1:BCB/SiO_2	3.2	86	15.5	3.1 ± 0.2	-1.5 ± 0.3	-0.1 ± 0.4	0.5 ± 0.1	10
T2:PS/SiO_2	2.9	84	15.3	2.1 ± 0.1	-0.1 ± 1.4	1.2 ± 1.3	0.5 ± 0.2	6
T3:PMMA/SiO_2	3.1	66	15.8	1.1 ± 0.1	1.4 ± 0.3	2.1 ± 0.4	0.4 ± 0.0	6
T4:OTS/SiO_2	4.1	98	16.6	1.2 ± 0.1	-0.8 ± 0.3	1.8 ± 0.6	0.6 ± 0.1	2

rms: root-mean-square roughness (of the substrates), Θ: contact angle, C_{OX}: capacitance density, μ: field-effect mobility, V_{TO}: turn-on voltage, V_T: threshold voltage, S: subthreshold slope, $I_{on/off}$: on/off current ratio.

4.1.3 Operational Stability Under dc Stress

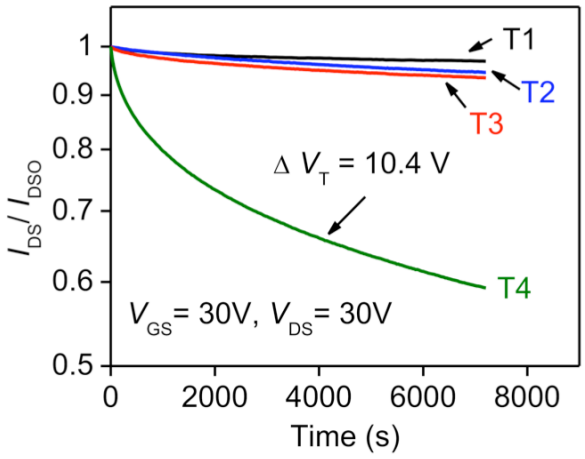


Figure 4.4: Time-dependent decay of I_{DS} of C_{60} OFETs for transistors T1 to T4 with different buffer layers under continuous dc biases of V_{GS} = V_{DS} = 30 V for 2 h. Transistor T4 (with OTS) shows a large threshold voltage shift of 10.4 V.

Also shown in Figure 4.3 (a) through (d) is the influence of the surface dielectric properties on the hysteresis sometimes observed in the transfer characteristics. Here, the threshold voltage shift (TVS) [$\Delta V_T = \Delta V_T{}^R(reversescan) - \Delta V_T{}^F(forwardscan)$] was used as a metric to quantify the hysteresis and bias stress effects. A value of ΔV_T = 2.9 V due to hysteresis was observed in T4 with an OTS SAM as shown in Figure 4.3(d**)**. However, the hysteresis behavior was strongly suppressed in transistors T1, T2 and T3 where the SiO_2 surface was passivated with hydroxyl-free polymers such as BCB, PS, or PMMA. The same trend was also found when conducting dc bias stress tests. No degradation was observed in transistors other than T4 (OTS) when the devices were repeatedly stressed by measuring transfer characteristics in the saturation regime 100

times with a 2s waiting time between scans. Figure 4.4 shows the time-dependent decay of I_{DS} of C_{60} OFETs with different buffer layers under continuous dc biases of V_{GS} = V_{DS} = 30 V for 2 hours. The C_{60} OFETs with polymers as a buffer dielectric (T1, T2, and T3) show negligible degradation with 3.1 %, 5.4%, and 6.6% decrease in I_{DS}, respectively. In contrast, T4 (OTS) devices show a steep decay with a 40% decrease in I_{DS} and a large V_T shift of 10.6 V.

4.1.4 Uniformity

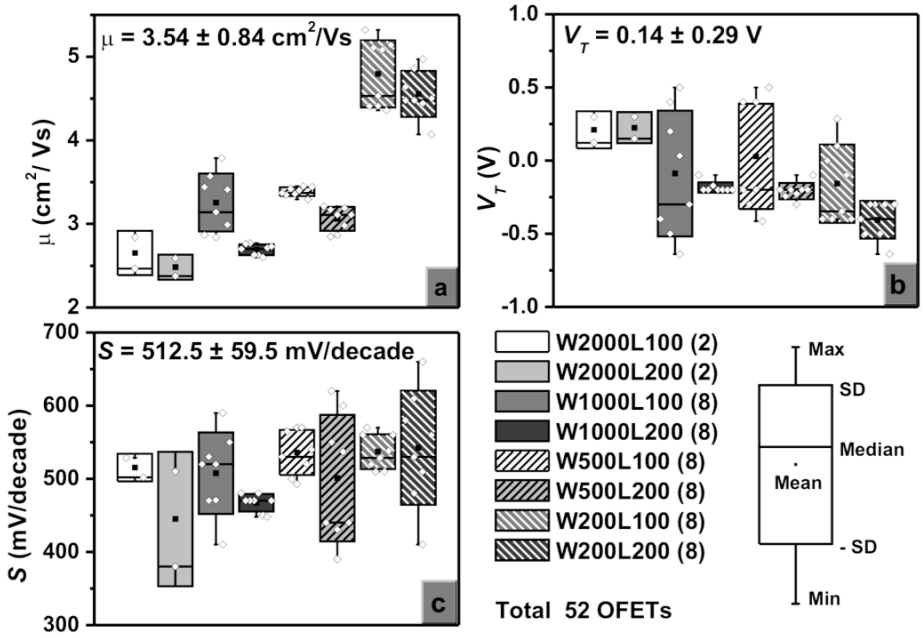


Figure 4.5: Statistical analyses of the electrical characteristics: mobility, threshold voltage, subthreshold slope of 52 C_{60} OFETs obtained from two substrates fabricated within the same batch.

In view of the best combination of performance and stability obtained in T1 devices, a set of 52 OFETs devices with channel width ranging from 200-2000 μm and channel

length of 100 or 200 μm was fabricated on two separate substrates that were processed identically within the same batch. The distribution and uniformity of device parameters (μ, V_T) measured in the devices are shown in Figure 4.5 in the form of box plots.

The on/off current ratios for the devices range from 10^6 to 10^8 where the resolution of the off current (10^{-11} A) is a limiting factor. The mobility values range from a minimum value of 2.7 cm^2/V s to a maximum value of 5.0 cm^2/V s with a mean value of 3.5 cm^2/V s and a SD of 0.8 cm^2/V s. Devices with the lowest W/L ratio ($W = L = 200$ μm) showed the highest mobility where geometry effects such as fringing currents may lead to larger effective field-effect mobilities. All the devices have a V_T near zero (0.1 ± 0.3 V) and a subthreshold slope S smaller than 1 (0.5 ± 0.1 V/decade).

4.1.5 Summary and Conclusions

Gate dielectrics modified by hydroxyl-free polymers show a significant improvement to the device stability. The nature of the gate dielectric surface plays an essential role in the device performance in addition to the C_{60} semiconductor itself. Our experimental results indicate the electrical instability of T4 transistors (with OTS) originates from charge trapping at or near the SiO_2 surface, where the surface silanol groups cannot be fully passivated by siloxane-based SAMs [128]. This finding is consistent with Chua's report [63] that the residual SiOH groups can capture/trap electrons and generate SiO^-/release H_2 when a positive gate bias is applied. However, the effects of various functional groups in the hydroxyl-free polymers on the electrical performance of C_{60} transistors are still not clear and will be further probed in our work.

In conclusion, we have demonstrated electrically stable, high-performance top-contact C_{60}-based *n*-channel OFETs in which BCB was inserted at the interface between

the semiconductor and the gate dielectric. Studies of electrical degradation under dc bias stress, performed on devices with different gate dielectric interfacial materials, have shown that hydroxyl-free polymers such as BCB, PS, and PMMA can lead to devices with superior lifetime in which interface charge trapping effects are minimized. Current devices were fabricated using PVD with substrates held at room temperature during the C_{60} deposition, demonstrating ease of processing over a large area. Testing was performed in an inert atmosphere at normal pressure. Future work will focus on passivating these transistors using ALD which provides good encapsulation as demonstrated recently with pentacene/C_{60} solar cells [68].

4.2 Reduction of Contact Resistance

As discussed previously, metals with low work functions are favored for electron injection. With low work-function contacts, better alignment and lower contact resistance between C_{60} and the source/drain electrodes can be achieved. Combining this concept with the results from Section 4.1, a device structure was designed using C_{60} as the semiconductor, hydroxyl-free BCB modified Al_2O_3 as the gate dielectric, and low work-function metal (i.e., Ca) as the source/drain electrodes. The active C_{60} layers were formed using physical vapor deposition (PVD) with the substrates kept at room temperature, which enables the fabrication of C_{60} devices and circuits on plastic substrates. The gate dielectric is essentially a dual-layer dielectric with Al_2O_3 to provide high capacitance and low-leakage, and a thin BCB buffering layer on top to provide properties compatible with C_{60}. The combination of Al_2O_3: BCB (gate dielectric) /C_{60} (semiconductor)/Ca (source/drain electrodes) as a device architecture not only enhances device performance

over a wide range of channel lengths at a low operating voltage, but also greatly improves the electrical stability and reproducibility.

4.2.1 Experimental Details

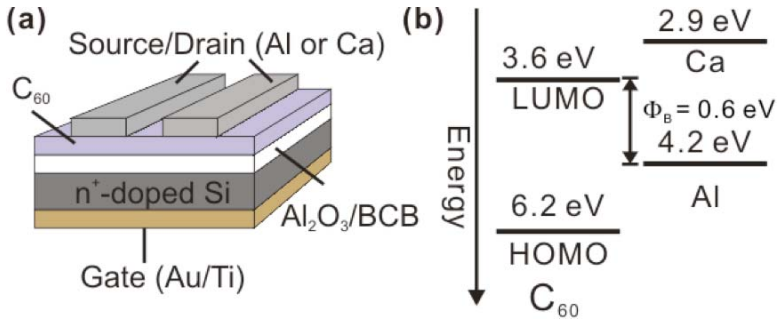


Figure 4.6: (a) Schematic of a C_{60} OFET with Al_2O_3/BCB dielectric and Al or Ca source/drain contacts. (b) Simplified energy band diagram of a C_{60} OFET at equilibrium (no biases applied) showing a Schottky contact formed at Al contact and C_{60} with a barrier height Φ_B of 0.6 eV.

With a top-contact geometry, as shown in Figure 4.6(a), OFETs were built on heavily *n*-doped silicon substrates (n^{++}-Si, $5 \times 10^{-3}\ \Omega$ cm) which was processed with a buffered oxide etchant (1:6 diluted HF in H_2O) to remove the native oxide. Ti/Au (10 nm/100 nm) metallization on the backside of the substrate was used to enhance the gate electrical contact. The front surface was coated with a 100 nm-thick layer of Al_2O_3 as the gate dielectric which was deposited at 100 °C by atomic layer deposition (ALD), a technique that allows for the deposition of highly conformal, defect-free dielectric layers at lower temperature [105]. The details of the gate dielectric film preparation have been published elsewhere [148].

To better control the interfacial properties between the dielectric and C_{60}, the Al_2O_3 dielectric surface was passivated with a thin buffer layer of BCB (Cyclotene^{TM}, Dow Chemicals). Crosslinkable BCB can provide a high-quality hydroxyl-free interface [63, 145] to the organic semiconductor with a high dielectric breakdown strength exceeding 3 MV/cm [137]. The thin buffer layers (c.a. 10 nm) were spin-coated from diluted Cyclotene^{TM} BCB and crosslinked at 250 ºC on a hot plate for 1 hour in a N_2-filled glovebox The total capacitance density (C_{OX}) measured from parallel-plate capacitors with 12 varying contact areas was 50 nF/cm^2. The leakage current density through the gate dielectrics was negligible (below 10^{-8} A/cm^2) under an applied field of 2 MVcm^{-1}.

Sublimed grade C_{60} (Alfa Aesar) was purified using gradient zone sublimation prior to deposition. A 50 nm-thick film of C_{60} was deposited at a rate of 0.6 Å/s using PVD at a constant pressure of 5×10^{-8} Torr while the substrates were held at room temperature. Subsequently, without breaking vacuum, 150 nm-thick top source/drain electrodes were deposited and patterned using a shadow mask. Devices had a wide range of width to length ratios, between 1 and 80, with channel lengths ranging from L = 25 μm to 200 μm and channel widths ranging from W = 200 μm to 2000 μm. With a low work-function of 2.9 eV, Ca was chosen for the source/drain electrodes to facilitate electron injection into the lowest unoccupied molecular orbital (LUMO) (3.6 eV) level of C_{60} [149, 150] since there is no barrier (Φ_B) between the C_{60} LUMO level and the Ca Fermi level (E_F) according to the conventional Mott-Schottky (MS) model, as shown in Figure 4.6(b). Control devices were also fabricated with aluminum (Al) as source/drain electrodes. In this case, a high barrier height of 0.6 eV is present for electron injection

due to the higher work function of 4.2 eV of Al. The electrical measurements were performed in a N_2-filled glovebox (O_2, H_2O < 0.1 ppm) at normal pressure (1 atm) in the dark using an Agilent E5272A source/monitor unit. All transistors, for which data are reported here, underwent the same fabrication process, measurement, and analysis steps.

4.2.2 Electrical Characterization

Electrical stability under repeated and continuous electrical stress has been a key issue in the accurate measurement, analysis, and prediction of electrical performance of discrete devices and integrated circuits. Previous studies from Chua [63] established that electron traps (especially $SiOH^-$ and OH^-) at the dielectric/semiconductor interface are responsible for electrical instability of *n*-channel OFETs and lead to hysteresis and threshold voltage shift under dc bias stress. *N*-channel OFETs with a large shift often exhibit high threshold voltage since a large positive gain-source voltage V_{GS} is needed to fill the traps. dc bias stress tests were conducted to demonstrate the stability of devices with Ca electrodes. The time-dependent decay of the drain-source current I_{DS} in C_{60} OFETs was less than 3% under continuous dc biases of $V_{GS} = V_{DS}$ (drain-source voltage) = 5 V for 2 hours, as seen in Figure 4.7(a). Neither current degradation nor threshold voltage shift was observed in the transfer characteristics when the devices were repeatedly measured 100 times with a 2s waiting time between scans, as shown in Figure 4.7(b).

The electrical stability shown here can be attributed to a low interface trap density at the interface between C_{60} and the gate dielectric. A maximum interfacial trap density can be estimated from Equation (14) [125, 127]. The trap density at the interface with

BCB is calculated to be near or below 10^{12} $cm^{-2}\,V^{-1}$ with average values of *S* below 0.3 V/decade. This value is lower than the best values reported for OFETs [125, 139].

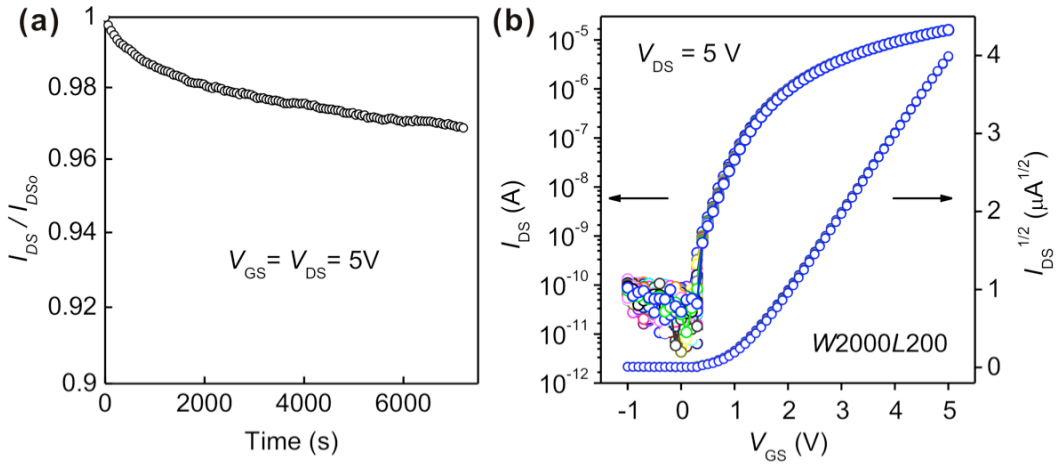


Figure 4.7: (a) Time-dependent decay of I_{DS} of a C_{60} OFET with Ca as source/drain contacts. (b) Superimposed transfer curves of 100 cycles from a C_{60} OFET with Ca as source/drain contacts.

As reported in pentacene *p*-channel OFETs [151], a decrease in mobility with increasing gate voltage was observed in C_{60} OFETs, as shown in Figure 4.8(a). The field-effect mobility is found to be gate-dependent in both the linear regime and the saturation regime. Initially, the mobility increases almost linearly with gate bias and reaches a peak value where all the surface traps are filled and the contact resistance is minimized. In our devices, it only takes about 2 - 3 V to reach the peak. Unlike the constant mobility in idealized MOSFETs, the mobility falls off slightly due to surface scattering which slows down the carriers, a typical phenomenon observed in MOSFET devices [83]. The slight decrease in mobility at higher gate bias is also reflected in the transconductance g_m, as seen in Figure 4.8(b).

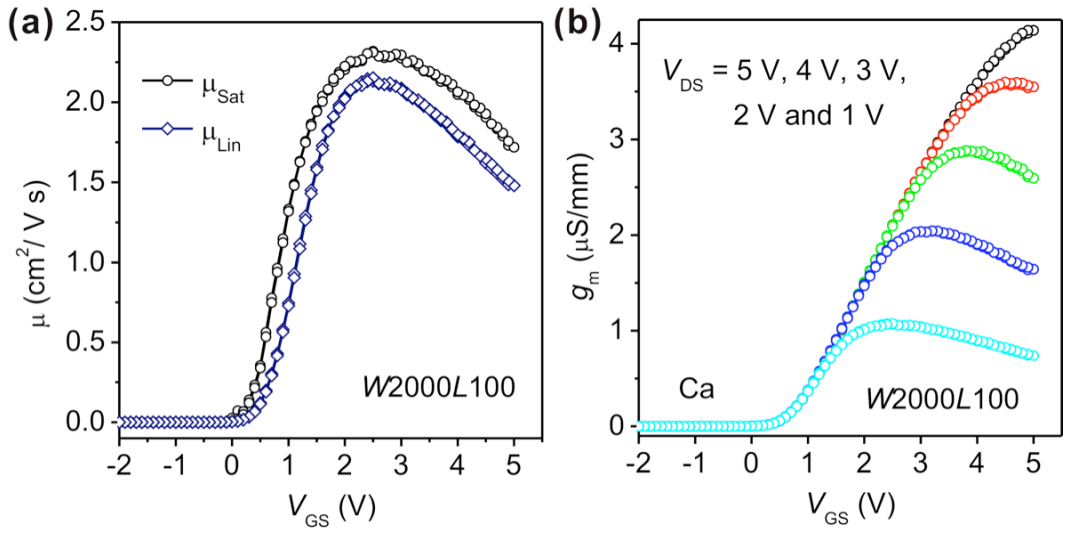


Figure 4.8: Mobility (a) and transconductance (b) degradation of a C_{60} OFET with Ca as source/drain contacts as a function of gate-source voltage V_{GS}. The mobilities were extracted both in the linear regime with V_{DS} = 1 V and in the saturation regime with V_{DS} = 5 V in a C_{60} OFET (L = 100 µm / W = 2000 µm).

In this work, the mobility peak values were used to characterize C_{60} OFETs while the surface scattering effects on the mobility are not discussed. The threshold voltage V_T was determined at the maximum of the second derivative of I_{DS} with respect to V_{GS} in the linear regime where V_{GS} of 5 V is much larger than V_{DS} of 0.05V. The V_T values calculated using this method are less sensitive to changes in both mobility and contact resistance [152].

Figure 4.9 (a) and (b) compare representative hysteretic transfer characteristics for both long-channel devices (L = 200 µm, Figure 4.9(a)) and short-channel devices (L = 25 µm, Figure 4.9(b)) with the same channel width W = 2000 µm and source/drain electrodes with Ca and Al, respectively. Representative output characteristics of C_{60} OFETs with Ca are shown in Figure 4.9(c) (L = 200 µm) and (d) (L = 25 µm).

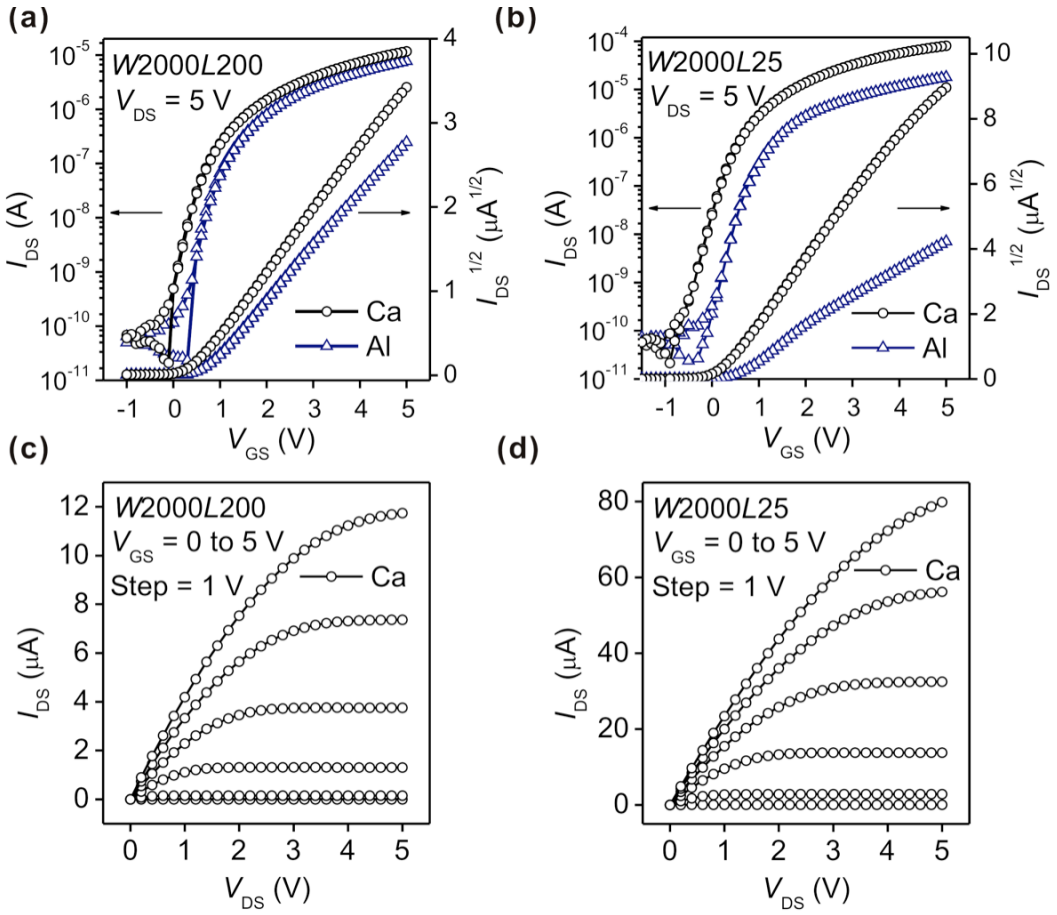


Figure 4.9: (a) and (b) Comparison of hysteretic transfer characteristics of both long-channel (*L* = 200 µm / *W* = 2000 µm) and short-channel (*L* = 25 µm / *W* = 2000 µm) C_{60} OFETs with Ca or Al as source/drain contacts. (c) and (d) Output characteristics of both long-channel and short-channel C_{60} OFETs with Ca as source/drain contacts.

The electrical parameters: field-effective mobility (μ), threshold voltage (V_T), subthreshold slope (S) and on/off current ratio ($I_{on/off}$) are summarized and compared in Table 5. For each type of transistor, 2 to 4 devices with identical geometry were measured to obtain a mean value and standard deviation (s. d.). As shown previously by our group [145], when using hydroxyl-free and high-purity BCB polymer to modify the dielectric interface, C_{60} OFETs presented no hysteresis and threshold voltage shift during

hysteretic gate bias scans. For long-channel devices (W = 2000 μm / L = 200 μm) as shown in Figure 4.9(a), devices with both Ca and Al electrodes show excellent performance with a V_T close to zero and S around 0.1 V/decade, while the mobility μ with Ca (2.3 ± 0.2 cm^2/Vs) is slightly higher than with Al (1.7 ± 0.1 cm^2/Vs). In contrast, when the channel length is scaled down to 25 μm, both devices start to show short-channel effects, such as a less pronounced saturation of I_{DS}, earlier turn-on, and higher subthreshold slope [103], as shown in Figure 4.9(b). However, while the devices with Ca contacts remain unaffected in mobility, the field-effect mobility for the devices with Al is greatly reduced to 0.4 cm^2/Vs in devices with shorter channels.

Table 5: Summary of the electrical parameters for C_{60} OFETs.

	S/D	μ (cm^2/Vs)	V_T (Volts)	S (V/dec)	$I_{on/off}$ ($\times 10^6$)
***W*2000*L*200**	Al	1.7 ± 0.1	0.3 ± 0.1	0.1 ± 0.02	0.4 ± 0.1
(*W*/*L* = 10)	Ca	2.3 ± 0.2	0.2 ± 0.1	0.1 ± 0.04	1.0 ± 0.3
***W*2000*L*25**	Al	0.4 ± 0.05	0.2 ± 0.1	0.3 ± 0.06	1.0 ± 0.2
(*W*/*L* = 80)	Ca	2.3 ± 0.1	0.1 ± 0.1	0.3 ± 0.03	4.0 ± 0.3

Each data point represents the mean value and the standard deviation (s.d.) calculated from 2 identical devices. S/D stands for source/drain electrodes. μ: field-effect mobility, V_T: threshold voltage, S: subthreshold slope, $I_{on/off}$: on/off current ratio.

4.2.3 Channel Length Scaling and Contact Resistance

To investigate the dependence of mobility on channel length L, field-effect mobilities of devices are statistically plotted over the inverse of channel length (L^{-1}) with channel width W = 500 μm, 1000 μm, and 2000 μm in Figure 4.10(a) and W = 200 μm in Figure 4.10(b).

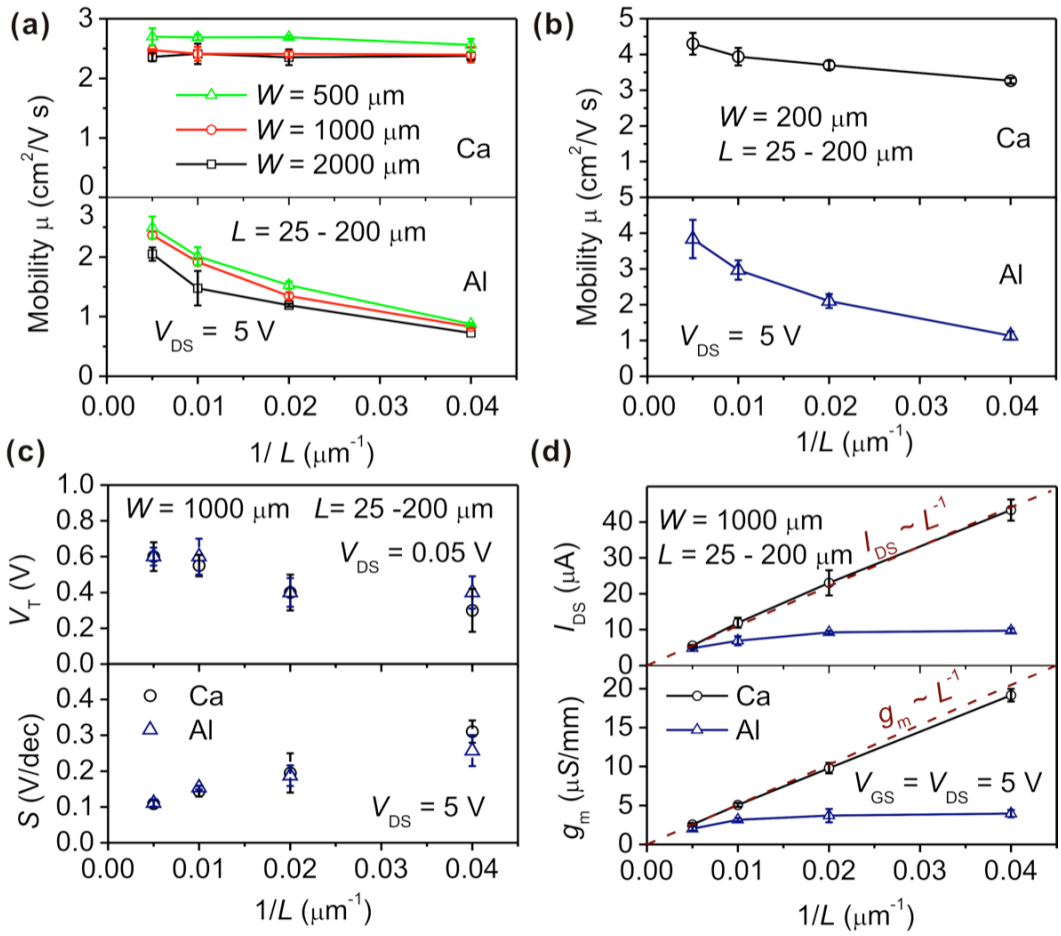


Figure 4.10: Effect of channel scaling on mobility μ [(a) and (b)], threshold voltage and subthreshold slope (c), drain-source current I_{DS} and transconductance g_m (d) in *n*-channel C_{60} OFETs with different source/drain contacts: Ca or Al. Each data point represents the mean value and the error bars represent the standard deviation (s.d.) calculated from 2- 4 identical devices (2 for W = 2000 μm and 4 for others).

In devices with Al as the source/drain electrodes, the mobility is greatly reduced with narrowing channel length. This is characteristic of many organic transistors since the carrier injection current is often primarily contact-limited due to the large Schottky barrier at the metal/organic interface, especially in *n*-channel OFETs. The Schottky

barrier is removed when Ca is used for the source/drain electrodes. The mobility for devices with Ca thus becomes independent of channel length in the range of L = 200 μm down to 25 μm. However, it is worth mentioning that the mobility values become exceptionally high (up to 4.5 cm^2/Vs) for devices with a channel $W = L$ = 200 μm where fringe current may lead to higher effective mobility, as seen in Figure 4.10(b).

In the case of V_T and S, as shown in Figure 4.10(c), the values do not scale with channel length as mobility does, but they do change slightly with decreasing channel length due to the higher transverse electric field in shorter channels. The field-effect current I_{DS} and transconductance g_m as a function of the inverse of channel length (L^{-1}) are also plotted and compared to those of devices with Al electrodes in Figure 4.10(d). With I_{DS} and g_m starting from similar values at L = 200 μm, devices with Al electrodes show typical contact-limited current where I_{DS} saturates and stops growing with decreasing channel length, while devices with Ca as the source/drain contacts show channel scaling with MOSFET-like characteristics where I_{DS} and g_m are proportional to L^{-1} with g_m larger than 15 μS/mm achieved for the short-channel devices with L = 25 μm.

To gain a better understanding of effect of the contacts on the mobility, the contact resistance of each metal with C_{60} was extracted using a transmission line method (TLM) based on the dependence of current-voltage characteristics on channel length, as described in section 2.2. According to Equations (12) and (13), the total width-normalized contact resistance $R_C W$ was extracted by plotting the width-normalized $R_{on} W$ as a function of L for different gate voltages, as shown in Figure 4.11(a). A set of devices with channel lengths ranging from L = 25 μm to 200 μm and a fixed channel width of W = 1000 μm was used to calculate the contact resistance at a low drain-source voltage

(V_{DS}) of 0.01 V for V_{GS} values ranging from 1 V to 5 V. By extrapolating $R_{on}W$ to L = 0 μm, the y intercept of the least squares fit yields $R_C W$ and the slopes correspond to sheet channel resistance R_{sh}. The width-normalized contact resistance ($R_C W$) and the sheet channel resistance (R_{sh}) of C_{60} transistors with Ca or Al contacts are shown in Figure 4.11(b) and (c), respectively. Similar to reports from many different groups [139, 153-155], the contact resistance with Al electrodes is strongly dependent on V_{GS} as seen from Figure 4.11(b) with a contact resistance of 20 kΩ-cm at V_{GS} = 5 V.

In general, there are two contributions to contact resistance in top-contact OFETs: the resistance of the metal contact/organic interface and the resistance of the organic film itself from the metal to the channel. The former can be reduced by tuning the Fermi level (E_F) of the metal with V_{GS} to lower the injection barrier, and the latter can be reduced by increasing the induced charge density in the accumulation regime with V_{GS}. In the case of Ca, the contact resistance drops drastically and rapidly reaches a constant value of 2 kΩ-cm by applying only 2.6 V, which is in contrast to the tens of volts needed for most OFETs. The residual contact resistance (which is no longer modulated by the gate bias) could be governed by the intrinsic conductivity of the C_{60} film. The low residual contact resistance achieved at extremely low V_{GS} is attributed to the combination of a low injection barrier between C_{60} and Ca and the high intrinsic mobility of C_{60} (therefore high conductivity). These findings are of significance in guiding the design of complementary circuits, especially when the inferior performance of *n*-channel OFETs is a limiting factor primarily due to their large contact resistance.

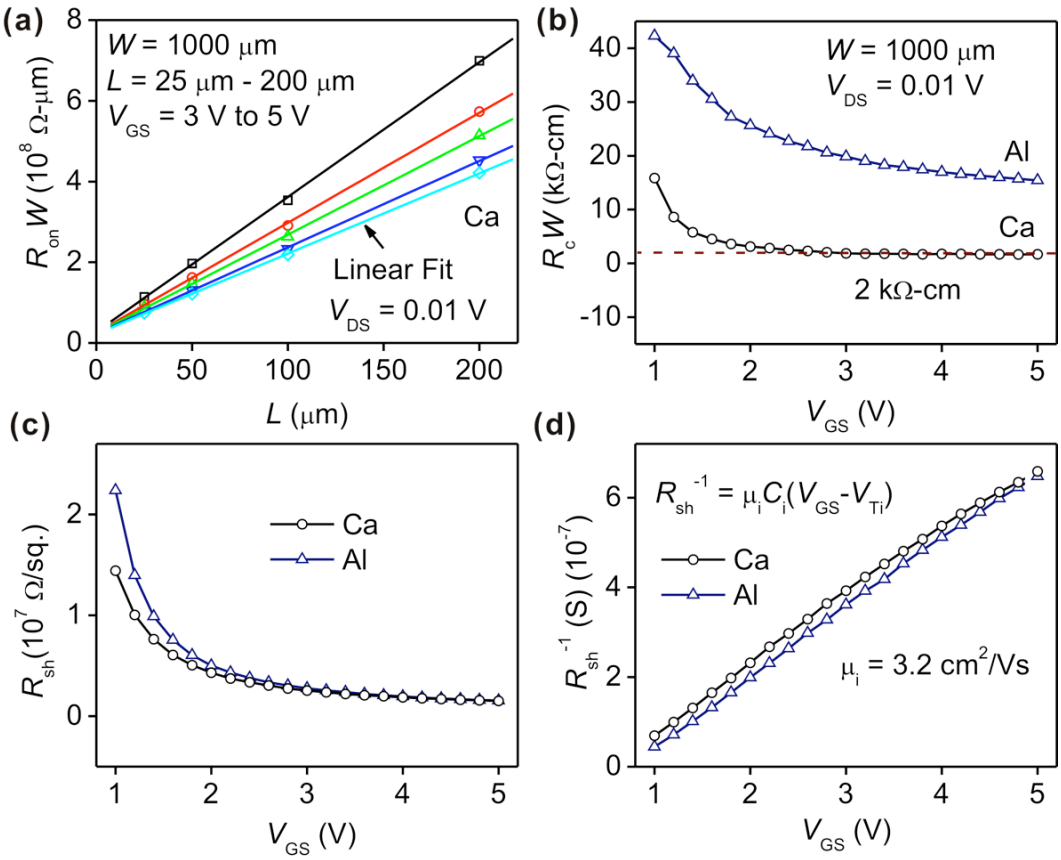


Figure 4.11: Total width-normalized contact resistance $R_{on}W$ (a), width-normalized contact resistance R_CW (b), sheet channel resistance R_{sh} (c), and sheet channel conductance R_{sh}^{-1} (d) of C_{60} OFETs shown as a function of gate-source voltage V_{GS} for a drain-source voltage V_{DS} = 0.01 V.

As shown in Figure 4.11(c), the sheet channel resistance R_{sh} is decreased when increasing V_{GS} due to an increase of induced charge density in the channel. According to Eq. (4), a corrected mobility (μ_c) from the contact resistance can be calculated from the slope of the linear least-square fit of R_{sh}^{-1}, which is equivalent to the channel sheet conductance, as shown Figure 4.11(d). As expected, since the C_{60} films were deposited during the same deposition run, a similar mobility of 3.2 cm^2/V s is obtained for both types of devices with Ca and Al as source/drain electrodes after the mobility is corrected

for the contact resistance. From these calculations, using devices with a channel width of W = 2000 μm (see Table 5) as an example, we can assess that the contact resistance from the C_{60} film accounts for a mobility degradation of less than 30%, from 3.2 to 2.3 cm^2/V s for Ca devices. On the other hand, the high injection barrier for Al devices account for an additional mobility degradation of more than 60%, from 3.2 to 0.4 cm^2/V s in short-channel devices with L = 25 μm. Consequently, the critical channel length, where the contact resistance starts to dominate, is calculated to be L = 100 μm with Al and only 10 μm with Ca. The latter is similar to the best results obtained from top-contact OFETs with pentacene and Au [139].

4.2.4 Conclusions

In summary, high-performance *n*-channel C_{60}-based OFETs with MOSFET-like electrical characteristics were fabricated. High electron mobilities (2.3 cm^2/V s for high W/L ratios and up to 4.3 cm^2/V s for low W/L ratios), threshold voltages near zero ($V_T < 1$ V), low subthreshold slopes ($S < 0.3$ V/decade), on/off current ratios larger than 10^6, and a maximum transconductance g_m larger than 15 μS/mm, along with excellent electrical stability under multiple test cycles (100 times) and continuous electrical stress were demonstrated. These combined properties were obtained by engineering the dielectric/organic semiconductor interface and by reducing the contact resistance at the metal contact/organic semiconductor interface. A mobility of 3.2 cm^2/V s corrected for contact resistance is shown to be independent of the nature of the metal contact. In addition, the electrical hysteresis/instability has been significantly reduced to a level where the OFETs exhibit excellent reproducibility and superior lifetime. Due to the

sensitivity of both the C_{60} semiconductor and the Ca electrode to ambient conditions, these devices will require encapsulation to protect them from oxygen and moisture.

CHAPTER 5 INTEGRATION OF N- AND P-CHANNEL OFETS: COMPLEMENTARY INVERTERS

In Chapter 3 and Chapter 4, we established proper interface engineering strategies at the dielectric/semiconductor to obtain both *p*-channel and *n*-channel OFETs with high electrical performance, low operation voltage, and good operational stability. In order to incorporate these OFETs onto the same substrate for inverters, one dielectric surface, which is compatible with both *p*-type and *n*-type semiconductors (pentacene and C_{60} in this work), is necessary to avoid complicated patterning procedures. Among the dielectric surface modification materials investigated for pentacene *p*-channel OFETs, both PS and BCB can provide a smooth dielectric surface with less trapping sites, which prompts the formation of an orderly, polycrystalline structure in pentacene films. Despite the high mobility and low threshold voltage in pentacene OFETs with BCB at the dielectric surface, the BCB surface yields poor operational stability probably due to the *p*-transport trapping molecules present in the BCB formulation as an antioxidant. In the case of C_{60} OFETs, both BCB and PS provide high electrical performance and excellent operational stability with BCB showing the best overall results. Considering the results from both *p*-channel and *n*-channel OFETs, PS is selected to modify the dielectric surface in the fabrication of organic complementary inverters. As far as gate insulators, Al_2O_3 deposited by ALD is used as a high-κ dielectric to provide both high capacitance density and low leakage current. The details regarding the deposition process by ALD have been thoroughly illustrated in the previous chapters.

Another major obstacle in the development of organic complementary circuits is the high contact resistance in OFETs, especially in *n*-channel OFETs. We adjusted the deposition condition for Au to achieve low contact resistance for pentacene *p*-channel OFETs, as described in Chapter 3. In Chapter 4, we employed Ca, a low work function metal, as source/drain electrodes to effectively lower the injection barrier between the electrodes and C_{60}. In this work, an issue regarding the air stability of OFETs and inverters is discussed and preliminary research on the encapsulation with a protective layer is conducted.

Section 5.1 covers the device structure and operation, and the basic design of organic complementary circuits. The characterization of static complementary inverters, including noise margins, switching voltage and dc gain, is also introduced. Then, flexible organic complementary inverters fabricated on a plastic substrate are demonstrated, as described in section 5.2. The flexibility and mechanical stability of the inverters are tested under bending experiments. Preliminary results from the encapsulation of OFETs and inverters are presented in section 5.3.

5.1 Introduction

5.1.1 Device Structure and Design

The research work involves the integration of *n*-channel and *p*-channel OFETs with comparable performance into complementary inverters. After the proper gate dielectrics and source/drain electrodes were identified for both *n*- and *p*-channel OFETs as stated in the previous chapters, the integration of two types of OFETs can be implemented by

fabricating the devices on one substrate with a combination of dielectrics and the source/drain electrodes that are compatible with C_{60} and pentacene.

In Chapter 4, we demonstrated low-voltage C_{60} *n*-channel OFETs with good electrical stability and low contact resistance [156]. To maintain operational stability for inverters, the interface of the gate insulator Al_2O_3 needs to be passivated with a smooth, trap-free dielectric layer that is stable for both *n*-channel and *p*-channel transport. In recent studies, as described in Chapter 3 and Chapter 4, we have found that a thin passivation layer of polystyrene (PS) at the gate dielectric/semiconductor interface provides high performance and good electrical stability not only for C_{60} OFETs [145], but also for pentacene OFETs. Material candidates for organic complementary inverters, as studied and identified from previous chapters, are listed in Table 6.

Table 6: Material candidates for organic complementary inverters.

	OSC	**Gate dielectrics**	**S/D**
***n*-channel OFETs**	C_{60}	Al_2O_3: PS	Ca
***p*-channel OFETs**	Pentacene	Al_2O_3: PS	Au

OSC: organic semiconductor; S/D: source/drain

The inverters are fabricated in a top-contact configuration, as shown in Figure 5.1 with connections between transistors (top view and cross section) and the corresponding circuit schematic. For convenience, the inverters use a common gate ($G_{n,p}$) for both *n*- and *p*-channel OFETs. This common gate is also the input node (V_{IN}) of the inverter. The drain terminals of the two OFETs ($D_{n,p}$) are connected to form the output node (V_{OUT}) of the inverter. The source of the *p*-channel OFETs (S_p) is connected to the supply voltage

(V_{DD}) while the source of the *n*-channel OFETs (S_n) is connected to the low power supply (V_{SS} = 0 V in this case).

The fabrication process involves the deposition of 6 layers as shown in Figure 5.1 with numbers for each layer showing the order of deposition. Among them, 4 layers, two organic semiconductors and the corresponding source/drain electrodes, are patterned using shadow masks.

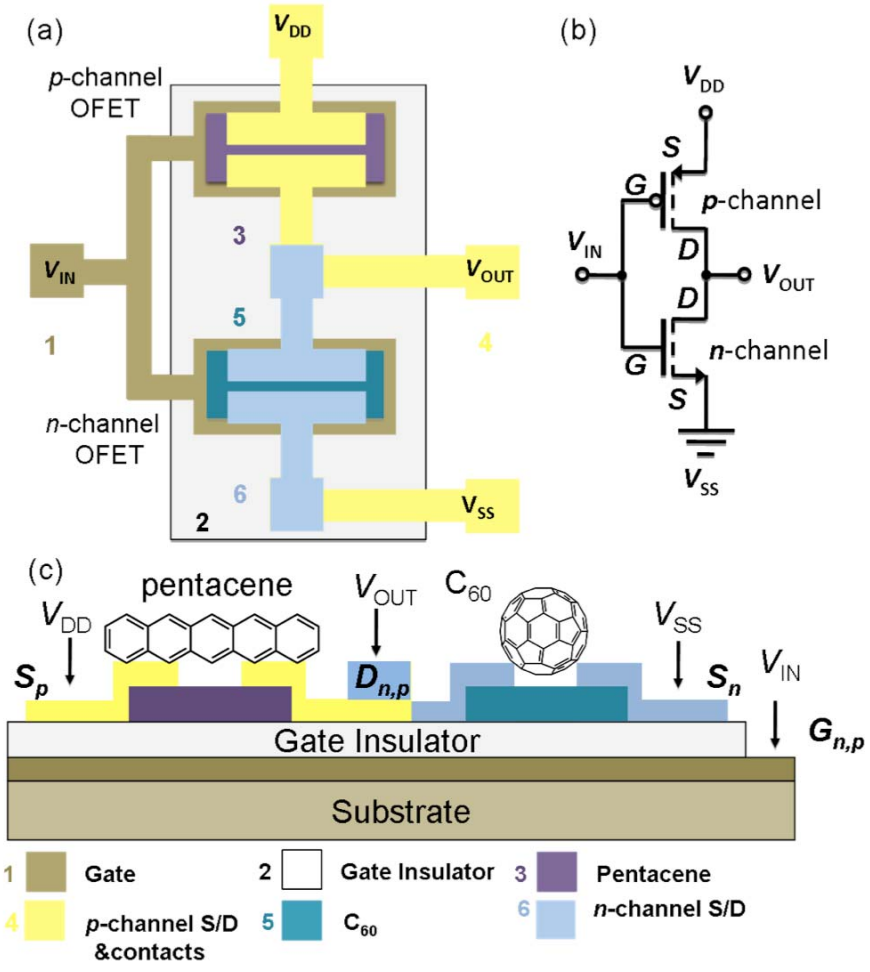


Figure 5.1: (a) top –view, (b) circuit diagram, and (c) side-view of of a CMOS inverter with C_{60} and pentacene as semiconductors.

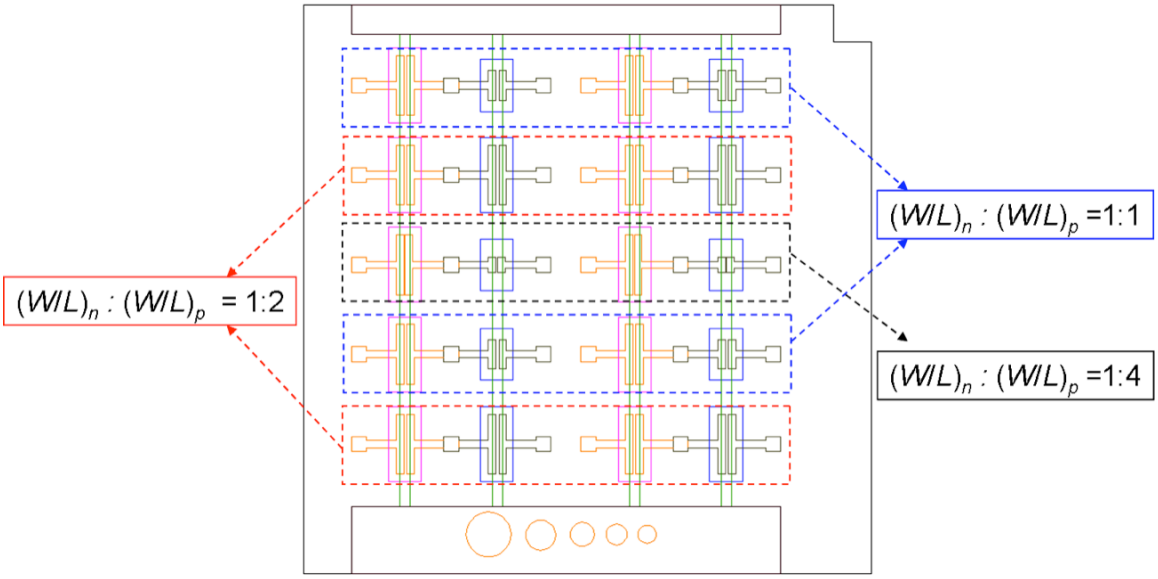


Figure 5.2: AutoCAD drawing of mask design for complementary inverters.

A set of 4 masks are designed and drawn using AutoCAD as shown in a top-view structure in Figure 5.2. The transistors have the same channel length with their channel width adjusted to accommodate the difference in the field effect mobilities. Since our *p*-channel pentacene OFETs show a mobility several times lower than that of n-channel C_{60} OFETs, the *W*/*L* ratio for *p*-channel is designed to be 4 times, 2 times, or equal to the *W*/*L* ratio for *n*-channel. More details on the design guides are illustrated in the next section.

5.1.2 Device Operation

The operation of a CMOS inverter [Figure 5.3(a)] can be readily understood from a simplified circuit model. The OFETs function in a manner similar to a switch with a finite on-resistance R_{on}. When V_{IN} is high (or equal to V_{DD}), the *n*-channel OFET is on (with a finite on-resistance R_{onn}), while the *p*-channel OFET is off (the switch is open), as

illustrated with an equivalent circuit in Figure 5.3(b). A conductive path is formed between the output node and the ground node, resulting in a low output voltage of 0 V. On the other hand, when the input is low (or equal to 0 V), the *p*-channel OFET is on and the *n*-channel OFET is off. The equivalent circuit in Figure 5.3(c) shows a conductive path between the supply voltage (V_{DD}) and the output voltage (V_{OUT}), leading to a high output voltage. There will never be a conducting path between the supply and ground under steady-state operation. Consequently, there is no static power consumption in CMOS inverters except for small power dissipation due to leakage current.

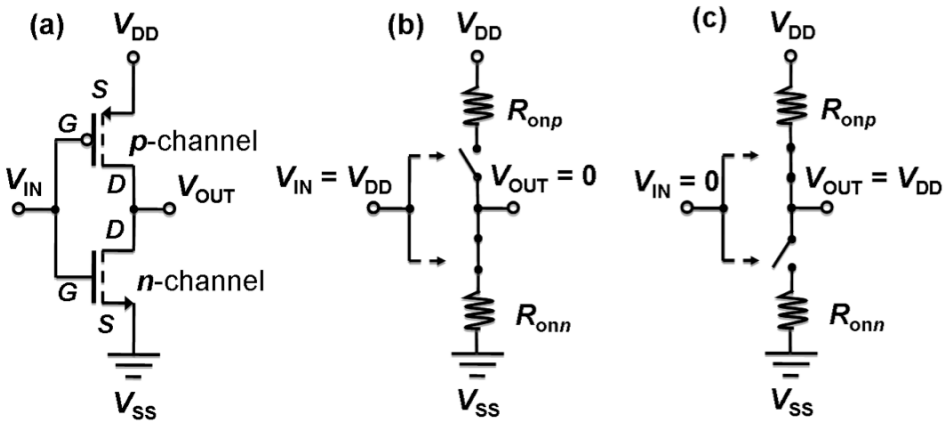


Figure 5.3: A CMOS inverter (a) and equivalent circuits for (b) high input and for (c) low input voltages.

A typical voltage transfer characteristic (VTC) of CMOS inverters is illustrated in Figure 5.4, which plots the output voltage (V_{OUT}) as a function of the input voltage (V_{IN}). The inverters are measured in a dark N_2-filled glovebox with the contacts connected as shown in Figure 5.3(a). The data acquisition is implemented using a Labview program. As denoted and listed in Table 7, five regions can be identified corresponding to different

operating conditions of each transistor. The details of these operating regions are explained elsewhere [58, 60]. The switching performance of a CMOS inverter can be characterized by noise margin, switching threshold voltage, and signal gain based on the inverter's static behavior.

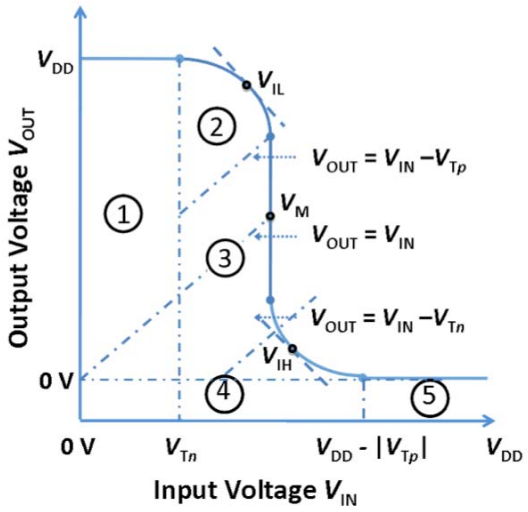


Figure 5.4: Voltage-transfer characteristics and operating regions of CMOS inverters.

Table 7: Operating regions of CMOS inverters

Regions	V_{IN}	V_{OUT}	*n*-OFET	*p*-OFET
1	$\leq V_{Tn}$	$V_{OH} = V_{DD}$	Cut-off	Linear
2	V_{IL}	High $\approx V_{OH}$	Saturation	Linear
3	V_M	V_M	Saturation	Saturation
4	V_{IH}	Low $\approx V_{OL}$	Linear	Saturation
5	$\geq V_{DD} - \lvert V_{Tp} \rvert$	$V_{OL} = 0$	Linear	Cut-off

5.1.3 Characterization of a Static Complementary Inverter

Noise Margins

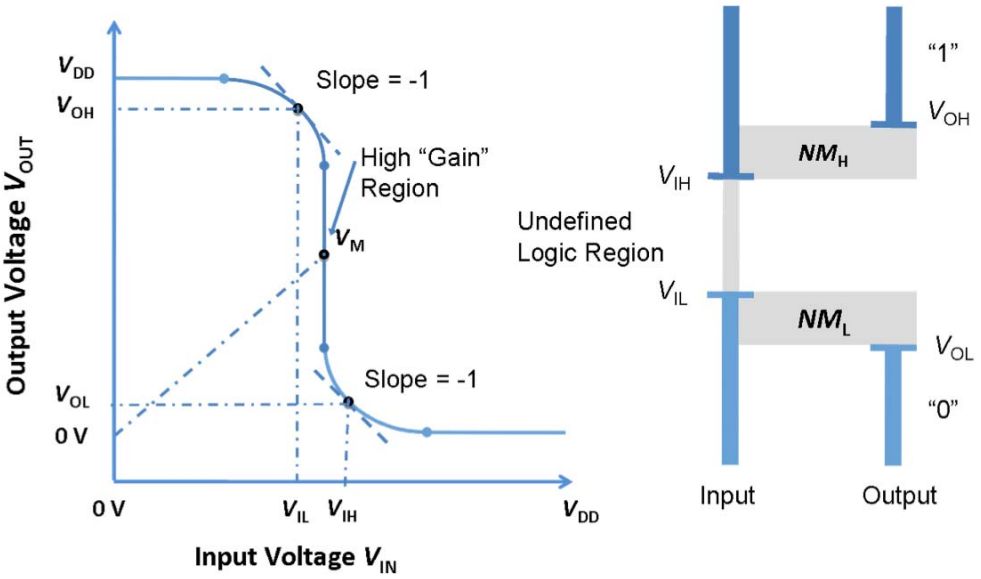


Figure 5.5: Definition of V_{IH} and V_{IL} and definition of noise margin (NM).

Noise margins represent the tolerance of the circuit to noisy inputs without generating erroneous output. The value of the margins should be larger than 0 for a functional digital circuit and preferably should be as large as possible. As illustrated in Figure 5.5, NM_L (noise margin low) and NM_H (noise margin high) are defined for low and high input levels using the following equations, respectively:

$NM_L = V_{IL} - V_{OL}$, and

$NM_H = V_{OH} - V_{IH}$, **(20)**

where V_{IL} represents the maximum input voltage that is recognized as a low input logic level, V_{IH} represents the maximum input voltage that is recognized as a high input logic level, and V_{OL} and V_{OH} are the output voltages corresponding to the input voltages of V_{IL} and V_{IH}, respectively. V_{IL} and V_{IH} are defined by the points where the gain ($g = dV_{OUT}/dV_{IN}$) of the VTC equals -1 as shown in Figure 5.5. In a well-behaved inverter, V_{OH} and V_{OL} are approximately equal to V_{DD} and 0 V, respectively.

The above analytic "textbook" approach is also referred as the negative slope criteria (NSC). Even though this is the primary analysis method used in this dissertation, it is worth mentioning some of its limitations and other alternative criteria. This criterion cannot prevent the maximum sum from occurring at points corresponding to zero or even negative noise margins. Another issue with NSC is that it cannot deal with the fact that the noise margins usually have multiple values.

One alternative criterion is to maximize the product of the two noise margins, referred as maximum product criteria (MPC). It can be graphically illustrated by maximizing the area of a rectangle embedded within the loop formed by the transfer curves of an inverter pair (i.e., VTC and its inverse), as shown in Figure 5.6(a). Any rectangle that can be embedded inside the loops represents a set of noise margins and corresponding V_{IL}, V_{IH}, V_{OL}, and V_{OH}. If the area of the rectangle is maximized, then the product of the two noise margins has been maximized. If the noise margins are forcibly equal and a square is maximized inside the inverter characteristic loop, as shown in Figure 5.6(b), then it is referred as the maximum equal criteria (MEC). For transfer curves that are nearly symmetric, the two criteria (MPC and MEC) give very close results.

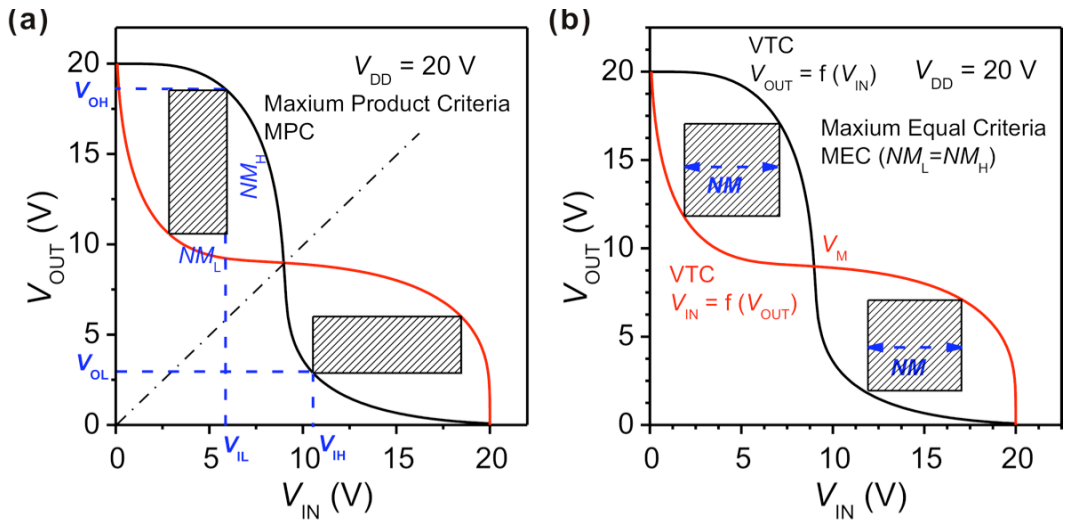


Figure 5.6: Illustrations of (a) the maximum product criteria (MPC) and (b) the maximum equal criteria (MEC).

Switching Threshold Voltage

The switching threshold voltage V_M is another important parameter that characterizes the steady-state input-output behavior of CMOS inverter circuits. V_M, defined as the point $V_{IN} = V_{OUT}$, can be identified graphically at the intersection of the VTC curve and the line given by $V_{IN} = V_{OUT}$, as seen in Figure 5.5. Setting the inverter threshold voltage to a desired voltage value is very important in the design of CMOS inverters.

For long-channel transistors, the channel-length modulation factor (λ) can be ignored. Then, the switching threshold voltage can be calculated from the performance parameters of the transistors [60]:

$$V_M = \frac{V_{DD} + V_{Tp} + \sqrt{k_R} \cdot V_{Tn}}{1 + \sqrt{k_R}} \quad \textbf{(21)}$$

where V_{Tn} and V_{Tp} are the threshold voltage of the *n*- and *p*-channel OFETs, respectively, and k_R is the ratio of the current gain factors ($k_p = k_n / k_p$) between *n*- and *p*-channel OFETs. The current gain factors are defined as follows:

$$k_p = \mu_p C_{OX} \left(\frac{W}{L} \right)_p$$
$$k_n = \mu_n C_{OX} \left(\frac{W}{L} \right)_n \quad \textbf{(22)}$$

where μ_n and μ_p are the mobility of *n*- and *p*-channel OFETs, respectively, and $(W/L)_n$ and $(W/L)_p$ are the width-length ratio of *n*- and *p*-channel OFETs, respectively.

Combining Equation (21) and (22), the ratio between $(W/L)_n$ and $(W/L)_p$ can be determined:

$$\frac{\left(\frac{W}{L} \right)_n}{\left(\frac{W}{L} \right)_p} = \frac{\mu_p}{\mu_n} \left(\frac{V_{DD} + V_{Tp} - V_M}{V_M - V_{Tn}} \right)^2 \quad \textbf{(23)}$$

Since the switching threshold voltage of an ideal inverter is defined as $V_M = \frac{1}{2} V_{DD}$, the calculation of size ratio can be further reduced to:

$$\frac{\left(\frac{W}{L} \right)_n}{\left(\frac{W}{L} \right)_p} = \frac{\mu_p}{\mu_n} \left(\frac{0.5V_{DD} + V_{Tp}}{0.5V_{DD} - V_{Tn}} \right)^2 \quad \textbf{(24)}$$

If the values of the threshold voltages are the same for the two transistors ($V_{Tn} = |V_{Tp}|$), then the inverter achieves a symmetric input-output characteristic. Then, Equation (24) can be further reduced as:

$$\frac{\left(\frac{W}{L}\right)_n}{\left(\frac{W}{L}\right)_p} = \frac{\mu_p}{\mu_n} \quad \textbf{(25)}$$

Equation (24) and (25) can serve as a guideline to determine the geometry of the transistors that can maximize the noise margins and obtain a symmetric characteristic.

dc Signal Gain

The signal gain of the inverters equals the gain (g) at the switching threshold V_M. A high gain in the transition region is very desirable. The gain $g = \frac{dV_{OUT}}{dV_{IN}}$ can be easily extracted from the VTC curve by calculating the derivative of V_{OUT} over V_{IN}. The gain primarily depends on the transconductances of the *n*- and *p*-channel OFETs at the midpoint voltage of the inverter. The static CMOS inverter can also be used as an analog amplifier, as it has a high gain in its transition region. This region, however, is very narrow as shown in Figure 5.5. The highest dc gain corresponds to the switching threshold voltage V_M.

5.2 Organic Complementary Inverters on Flexible Substrates

5.2.1 Experimental Details

The complementary inverters were built on a 75 μm-thick polyethylene naphthalate (PEN) substrate. Before use, the PEN film was pre-shrank by thermal annealing at 130 °C for several hours in a vacuum oven. The inverters were fabricated in a top-contact configuration, as shown in Figure 5.1(a) and (c) with connections between transistors leading to the corresponding circuit schematic shown in Figure 5.1(b). Source/drain

electrodes of Au for the *p*-channel and Ca for the *n*-channel transistors were selected to minimize the contact resistance. A 50 nm-thick layer of Au with a 10 nm-thick layer of Ti, serving as a common gate ($G_{n,p}$) for both the *n*- and *p*-channel OFETs, was deposited using an E-beam deposition system. This common gate also acts as the input node (V_{IN}) of the inverter. A 200 nm-thick Al_2O_3 gate insulator was formed by ALD at 100 °C as described elsewhere [148]. To better control the interfacial properties at the dielectric and C_{60}/pentacene, the Al_2O_3 dielectric surface was coated with a thin layer of PS to passivate the polar groups and impurities at the interface. PS films were spin-coated from a 4 mg/ml solution in toluene and annealed at 120 ºC on a hot plate for 1 h. After coating with PS, the dielectric surface turned hydrophobic with a water contact angle of 88°. The capacitance density C_{OX} was 26.5 nF/cm^2, measured from parallel-plate capacitors with 12 varying contact areas.

C_{60} (Alfa Aesar) and pentacene (Sigma-Aldrich) were purified by thermal gradient zone sublimation prior to deposition. The C_{60} (50 nm) and pentacene (50 nm) layers were deposited at a rate of 1 Å/s and 0.3 Å/s, respectively. The top-contact source/drain electrodes with Au (60 nm) for the *p*-channel and Ca (150 nm) for the *n*-channel OFETs were deposited at a rate of 1 Å/s. The substrates were held unheated during all the deposition processes with a chamber pressure below 5×10^{-8} Torr. The semiconductor layers and source/drain contacts were patterned by a set of shadow masks. Photographic images of the flexible inverters are shown in Figure 5.7.

As shown in the circuit diagram in Figure 5.1(b), the drain terminals of the two OFETs ($D_{n,p}$) were connected to form the output node (V_{OUT}) of the inverter. A supply voltage (V_{DD}) was applied to the source of the *p*-channel OFETs (S_p) while a low power

supply (V_{SS} = 0 V in this case) was applied to the source of *n*-channel OFETs (S_n). The electrical measurements were performed in a N_2-filled glovebox (O_2, H_2O < 0.1 ppm) at normal pressure (1 atm) in the dark using an Agilent E5272A source/monitor unit and an Agilent E3647A dc output power supply.

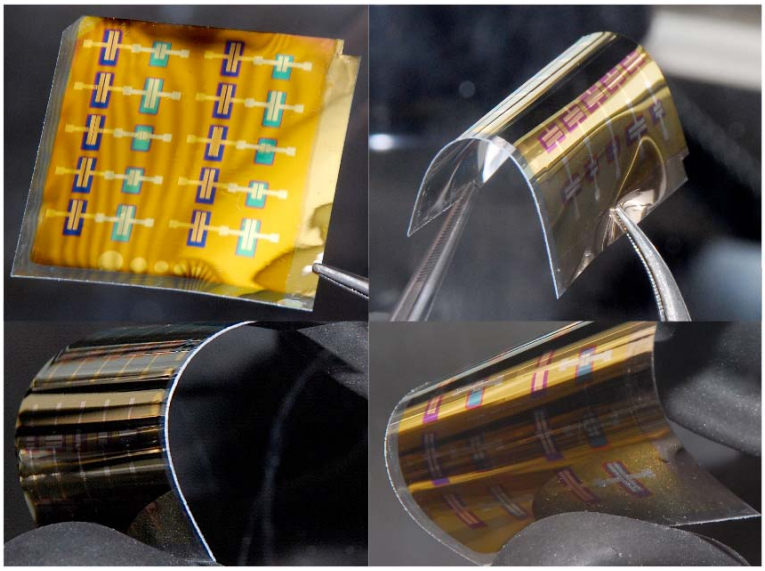


Figure 5.7: Photographic images of flexible organic complementary inverters.

5.2.2 Electrical Characterization

The current-voltage characteristics (i.e., output and transfer curves) of both *p*-channel and *n*-channel OFETs are shown in Figure 5.8(a-d). The output characteristics exhibit good ohmic-contact behavior for both *p*-channel [Figure 5.8 (a)] and *n*-channel OFETs [Figure 5.8 (c)] with I_{DS} increasing linearly with V_{DS} in the linear regime. The

transfer curves were measured for both forward and reverse gate bias as shown in Figure 5.8 (b) (*p*-channel) and Figure 5.8 (d) (*n*-channel).

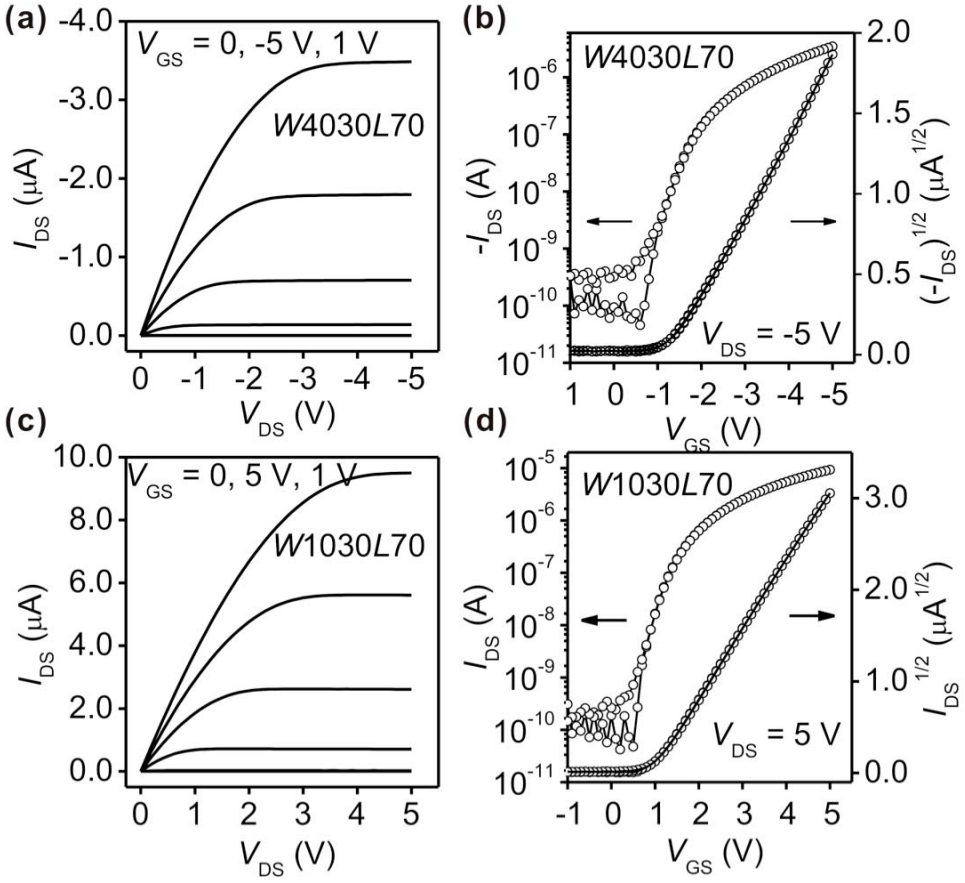


Figure 5.8: (a) Representative output and (b) hysteretic transfer curves for pentacene *p*-channel OFETs; (c) Representative output and (d) hysteretic transfer curves for C_{60} *n*-channel OFETs.

No threshold voltage shift or hysteresis was observed in either type of transistors, demonstrating good electrical stability with PS as the gate dielectric interface for both hole and electron transport. Field-effect mobilities μ and threshold voltages V_T were

calculated in the saturation regime using standard MOSFET models by fitting the $\sqrt{|I_{DS}|}$ vs V_{GS} data to a square law model. Also extracted from the transfer characteristics are subthreshold slope (S) and maximum channel on-current [I_{DS}(max)]. The extracted electrical parameters [μ, V_T, S, and I_{DS}(max)] (calculated from forward bias scans) are summarized and compared in Table 8.

Table 8: Summary of the electrical parameters for *p*-channel pentacene and *n*-channel C_{60} OFETs.

	W/L **(μm/μm)**	***μ*** **(cm^2/Vs)**	V_T **(V)**	***S*** **(V/dec)**	I_{DS} **(max) (μA)**
***p*-channel**	4030/70	0.33	-2.7	0.2	-3.5
***n*-channel**	1030/70	2.17	2.1	0.3	9.5

W/*L*, channel width/length; μ, field-effect mobility; V_T, threshold voltage; *S*, subthreshold slope; I_{DS}(max), maximum channel on-current.

C_{60} *n*-channel transistors show similar performance to the devices fabricated on rigid substrates [156] with a high mobility of 2.17 cm^2/Vs, a low threshold voltage V_T of 2.1 V, and a sharp subthreshold slope *S* of 0.3 V/dec. The pentacene *p*-channel transistors show a threshold voltage of -2.7 V and a subthreshold slope of 0.2 V/dec, which are comparable to those of the C_{60} transistors. However, the hole mobility (0.33 cm^2/V) is about 6 times lower than the electron mobility (2.17 cm^2/V s). The reduction of hole mobility on a plastic substrate was caused by the disturbed growth of the pentacene film

and the impedance of charge transport on the rough surface. The lower mobility of pentacene compared to C_{60} was partially compensated for by having a channel width of the *p*-channel OFET (W = 4030 μm) four times larger than that of the *n*-channel transistor (W = 1030 μm). A channel length L = 70 μm was used for both devices.

With low threshold voltages for both transistors, the inverters could be operated at a supply voltage as low as 3 V. The voltage transfer characteristics (VTC) with a supply voltage of V_{DD} = 3 V, 4 V, and 5 V are shown in Figure 5.9(a). The switching voltage V_M was obtained graphically from the intersection of the VTC with the line $V_{OUT} = V_{IN}$. V_M values are 2.4 V, 2 V, and 1.6 V corresponding to V_{DD} = 5V, 4 V, and 3 V. These numbers are very close or equal to the maximum theoretical values of 0.5 V_{DD}, showing a good symmetry of VTC due to the comparable threshold voltages in the individual *n*- and *p*-channel transistors.

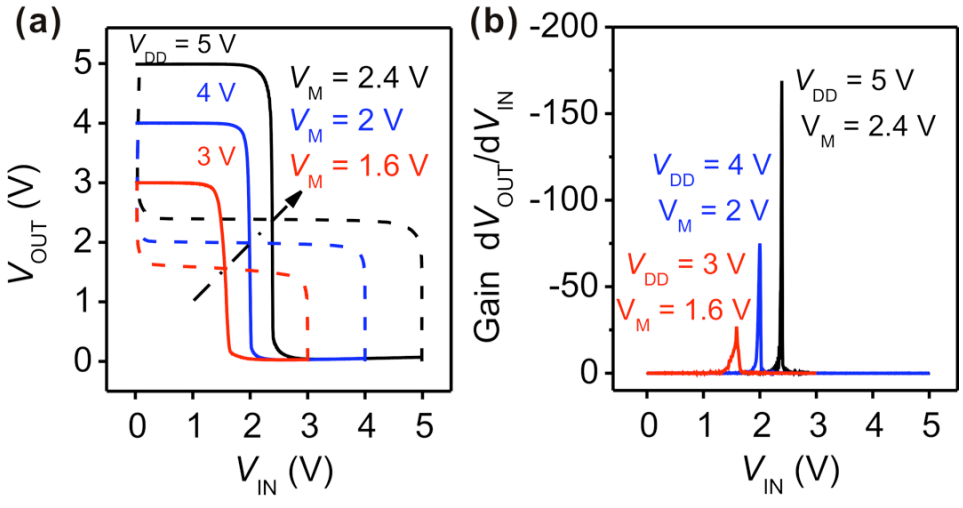


Figure 5.9: (a) Voltage transfer characteristics of a static organic complementary inverter; (b) corresponding calculated dc gain values.

The noise margin (*NM*) was characterized by the negative slope criteria [58]. The low noise margin (NM_L) and high noise margin (NM_H) are 2.0 V and 2.3 V for V_{DD} = 5 V, 1.7 V and 1.8 V for V_{DD} = 4 V, and 1.2 V and 1.2 V for V_{DD} = 3 V. Those values are higher than 80% of the maximum theoretical values of the noise margins ($NM_L = NM_H = 0.5V_{DD}$). To the best of our knowledge, these results are among the highest noise margin values obtained in organic complementary inverters. The maximum dc voltage gain, defined as dV_{OUT}/dV_{IN}, is dependent on V_{DD} as shown in Figure 5.9(b). A high dc gain of 180 was achieved with V_{DD} = 5 V. The V_{IN} values at the highest dc gains correspond to V_M values obtained in Figure 5.9(a).

5.2.3 Bending Experiment

The inverters were subjected to bending experiments to test their stability under flexing as illustrated in Figure 5.10(a). They were tested before bending (test #1), tested again after bending under a tensile stress (test #2, devices on the outer surface), and then tested after bending under a subsequent compressive stress (test #3, devices on the inner surface). During each bending test, the samples were first bent at a radius R = 5 mm, held in that position for 5 s, and released. This cycle was repeated 5 times. Since the thickness of the gate dielectric is negligible compared with the thickness of the substrate film (D = 75 μm), a strain ε = 0.75% for a bending radius of R = 5 mm can be approximated from the value of $D/2R$ [157, 158].

The changes to the transfer and output characteristics of individual OFETs induced by the bending are shown in Figure 5.10(b). The saturation current for the pentacene *p*-channel OFET decreased by only 0.6% after the tensile strain but increased by 4% after the compressive strain. This observation agrees well with Yang's report on bending-

stress-driven transitions in pentacene thin films [159]. On the other hand, the *n*-channel saturation current increased both with the tensile and compressive strains by 8% and 13%, respectively. With these changes in the individual transistors, the VTC of the inverter shifted by a negligible value of 0.6% under the tensile strain and by a small fraction of 3% under the compressive strain [Figure 5.10 (c)]. Accordingly, the maximum dc gain increased by 11% and 20 % for tensile and compressive stresses, respectively.

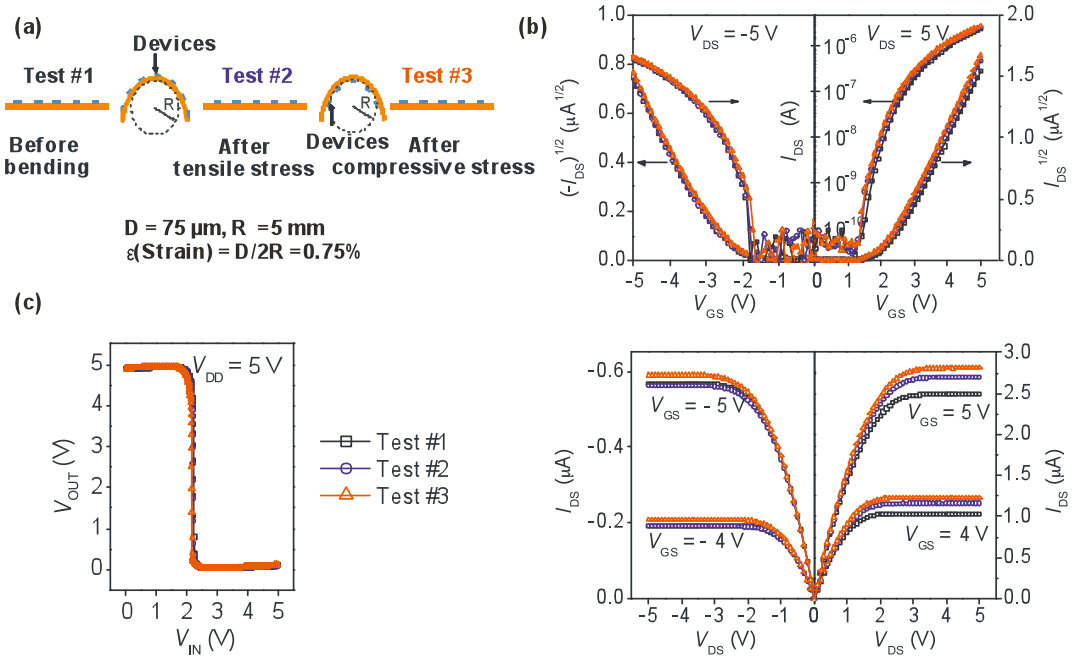


Figure 5.10: (a) Illustration of bending experiments with both tensile and compressive stresses. Superposition of (b) the transfer and output characteristics of *p*-channel and *n*-channel OFETs and of (c) the voltage transfer characteristics of the inverters measured before/after tensile and compressive stress cycles.

5.2.4 Conclusions

In summary, we have demonstrated organic flexible inverters with both high noise margin and high dc gain at low supply voltage. With the surface of the gate dielectrics

passivated with a thin layer of PS, both *n*-channel and *p*-channel OFETs show negligible hysteresis and comparable threshold voltages. The inverters can be operated at a supply voltage as low as 3 V with noise margin values higher than 80% of their maximum theoretical value. A high dc gain of 180 was obtained at a supply voltage of 5 V. The performance of flexible inverters did not degrade after bending; instead, a small increase in dc gains was observed.

5.3 Encapsulation of Organic Complementary Inverters: Preliminary Study

5.3.1 Introduction to Multilayer Thin-Film Encapsulation

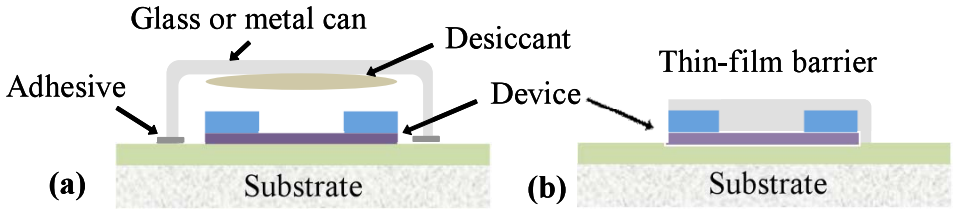


Figure 5.11: Schematic diagram for traditional (a) and thin-film (b) encapsulation structures.

As mentioned in the introduction of this dissertation, OFET devices must be encapsulated to provide longer operational lifetime due to the sensitivity of these electronics to the moisture and oxygen in the environment. The traditional encapsulation approach (especially for OLEDs) involves attaching a metal or glass lid to the substrate using a low-permeation adhesive [160], as shown in Figure 5.11(a**)**. A desiccant is often

incorporated to remove the byproduct from the adhesive drying process. This method is not compatible with flexible electronics due to the rigidity, weight, and cost of the lid. In contrast, thin-film encapsulation can protect these devices while maintaining both a flexible form factor and lightweight. This approach also gives lesser concern for abrasion damage from the lid during the bending of the flexible electronics, as shown in Figure 5.11(b**)**.

Inorganic films like oxides can be effectively impermeable to O_2 and H_2O, if made perfectly. However, there are always imperfections and defects caused by surface topography and particles introduced during deposition, leading to the permeation of H_2O and O_2 molecules through these paths. Polymer/inorganic multilayer structures have been shown to offer a significant improvement in permeation-barrier performance [160]. As shown in Figure 5.12, multiple inorganic oxide layers can provide good barriers and highly non-conformal polymer layers can decouple defects between layers.

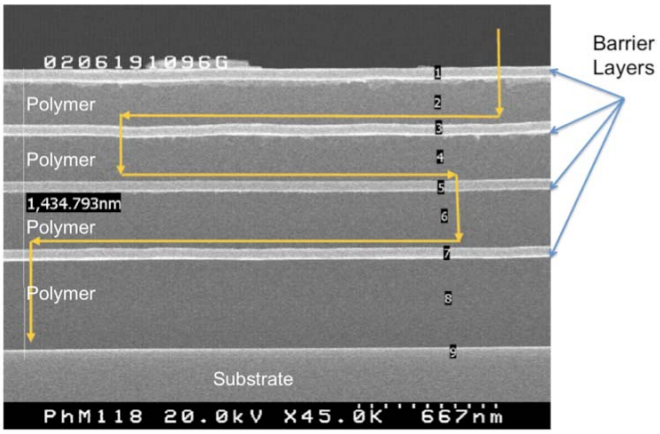


Figure 5.12: Polymer/inorganic multilayer structure from Vitexsys.

Using this approach, the “effective” diffusion path can be elongated (tortuous path) and the permeation rate can be reduced. Polymer films can also planarize/smooth the surface to reduce substrate defects. More layers can provide better encapsulation since the particles and topographic defects can be covered by redundantly using alternating layers of polymer and oxide.

The deposition process of thin-film barriers must, however, be compatible with the underlying devices to avoid damage to the devices. Contact of OFET devices with potential sources of damage, such as solvents, water, O_2, and sometimes plasmas, must be avoided to prevent deterioration of the active materials. Furthermore, the deposition temperature has to be relatively low, which often limits the quality of barrier films.

In the preliminary study, a multilayer structure of alternating layers of organic and oxide layers can be employed as an encapsulation layer for both *n*-channel and *p*-channel OFETs and the inverters. One candidate for the organic layer is poly-monochoro-*p*-xylylene (usually known as parylene-C). Deposited by chemical vapor deposition (CVD), parylene can form a smooth and uniform coating using a unique polymerization process instead of the use of solvents during vapor deposition. The advantage of this process is that the coating is formed from a gaseous monomer without an intermediate liquid stage; therefore, the polymerization can be performed at ambient temperature. This vapor-deposited polymer has also been used as the top-gate dielectric and even an encapsulation layer in pentacene OFETs [69, 161-163]. Al_2O_3, a high-density oxide widely used for encapsulation as a barrier layer, is deposited by ALD at a deposition temperature of 100 °C. The deposition condition for high-quality Al_2O_3 films as gate dielectric insulators with low leakage current has been studied in the previous research [148]. Al_2O_3 by ALD

has been demonstrated as a good encapsulation material for pentacene/C_{60} solar cells [68].

The systems for the deposition of parylene and Al_2O_3 are not incorporated into a N_2-filled glove box. The devices have to be exposed to atmospheric conditions between the depositions. Short-term exposure to O_2 and H_2O does not induce drastic performance degradation in *p*-channel pentacene OFETs. In the case of *n*-channel OFETs, the adverse effect of exposure can be disastrous. The electron injection and transport are hindered immediately after exposure to oxygen, even under reduced pressure, as shown in Figure 5.13(a). Within several minutes in air, the device channel current drops several orders of magnitude, as seen in Figure 5.13(b).

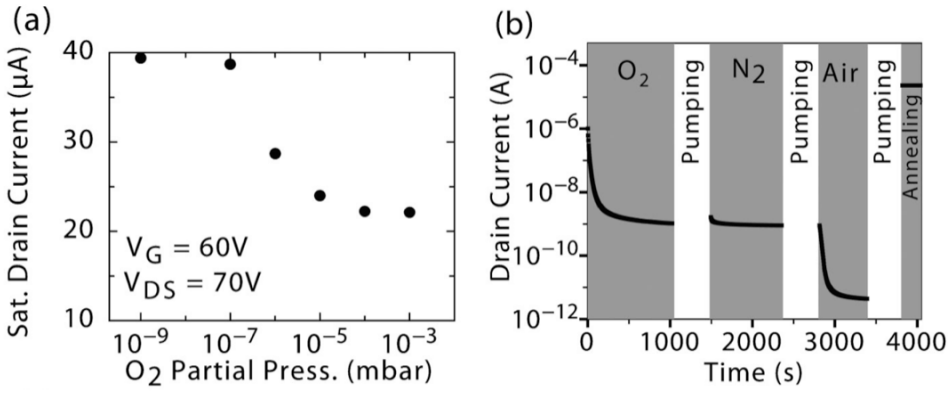


Figure 5.13: (a) Saturation drain current of a C_{60} OFET vs the partial pressure of a 2 min oxygen exposure. (b) Real-time observation of the degradation of the normalized drain current of a C_{60}-FET under sequential exposure to impurity gases at atmospheric pressure [164].

Furthermore, low work-function metals, such as Ca, are also very sensitive to H_2O and O_2, despite that they are favored as S/D electrodes since they form a lower injection barrier for electrons. For example, Ca is very reactive with H_2O and O_2 and forms

calcium salt. The reaction is so sensitive that it has been used to test the permeation rate of H_2O or O_2 by testing the change of resistance or optical transmission [165, 166]. In some cases, even though the reaction does not cause the complete loss of conductivity of Ca, the contact resistance will become so large that the devices cannot function properly without applying high voltage.

Due to the above reasons, it becomes critical to protect the devices with a buffering layer prior to the encapsulation process. The desirable material for a buffering layer has to fulfill at least three requirements: first, it can be deposited onto the devices without causing initial damage; second, it can be formed in a system where the devices will not be exposed to air during handling; third, it can prevent any further damage to the active layers from the following encapsulation process. In this work, we used tetratetracontane (TTC) ($C_{44}H_{90}$) as a protective material for pentacene, C_{60} and Ca. TTC has been demonstrated as a good passivation material for pentacene OFETs [167]. It can be easily deposited using a thermal evaporator and can form a hydrophobic, closely packed, and crystalline layer. The preliminary study on the encapsulation of the inverters explores the possibility of encapsulating OFETs effectively, especially *n*-channel devices, to justify the practicality of organic complementary circuits. The work focuses on the usage of a protective layer to prevent the devices from further damage from the encapsulation. As long as the device is well protected at this step, the encapsulation process can adopt similar procedures for OLED passivation, as developed for consumer electronics. The encapsulation process itself involves many complicated steps, such as attaching external contacts, depositing multi-layers, sealing edges, testing in a controlled environment, etc.

The detailed encapsulation process is not, but the protective layer is, within the scope of this dissertation: Interface engineering towards organic complementary inverters.

5.3.2 Experimental Details

The fabrication process of inverters is very similar to the description in section 5.1 and 5.2 with pentacene and C_{60} as active semiconductors, except that the inverters were built on a rigid substrate. The inverters were built on n^{++}-Si substrates with n^{++}-Si as a common gate ($G_{n,p}$) for the both *n*- and *p*-channel OFETs; therefore, the n^{++}-Si serves as the input node (V_{IN}) for the inverter. A thinner Al_2O_3 (100 nm) layer deposited by ALD was used as a gate insulator and its capacitance density is about 43 nF/cm^2 with a thin layer of PS coated at the surface. After the fabrication, the inverters were first tested without exposure to air. Then the sample went through a different encapsulation process described by the following. Sample A was directly encapsulated with 200 nm-thick Al_2O_3 deposited by ALD. Sample B and C were loaded back into the Spectros for the deposition of a protective layer with TTC. Then, Sample C was further coated with a layer of Al_2O_3. All layers were blanket-coated on the substrate without patterning, external contacts, and edge seals. Al_2O_3 was deposited using an ALD system which is not attached to a N_2-filled glove box, so the samples had to be briefly exposed to air for about 2 min during the handling. The substrate temperature was 100 °C and a chamber pressure as low as 10^{-3} torr was achieved with a mechanical rough pump. The TTC layer was deposited in a Spectros, a thermal evaporator, which is the same system used for the deposition of the inverters. The deposition was performed under a chamber pressure of 5×10^{-8} Torr and with a deposition rate of 10 Å/s where the substrate was held at room temperature. After

encapsulation, sample A, B and C were loaded back into a N_2-filled glove box for electrical testing. A brief exposure to air occurred during the transfer.

5.3.3 Results and Discussions

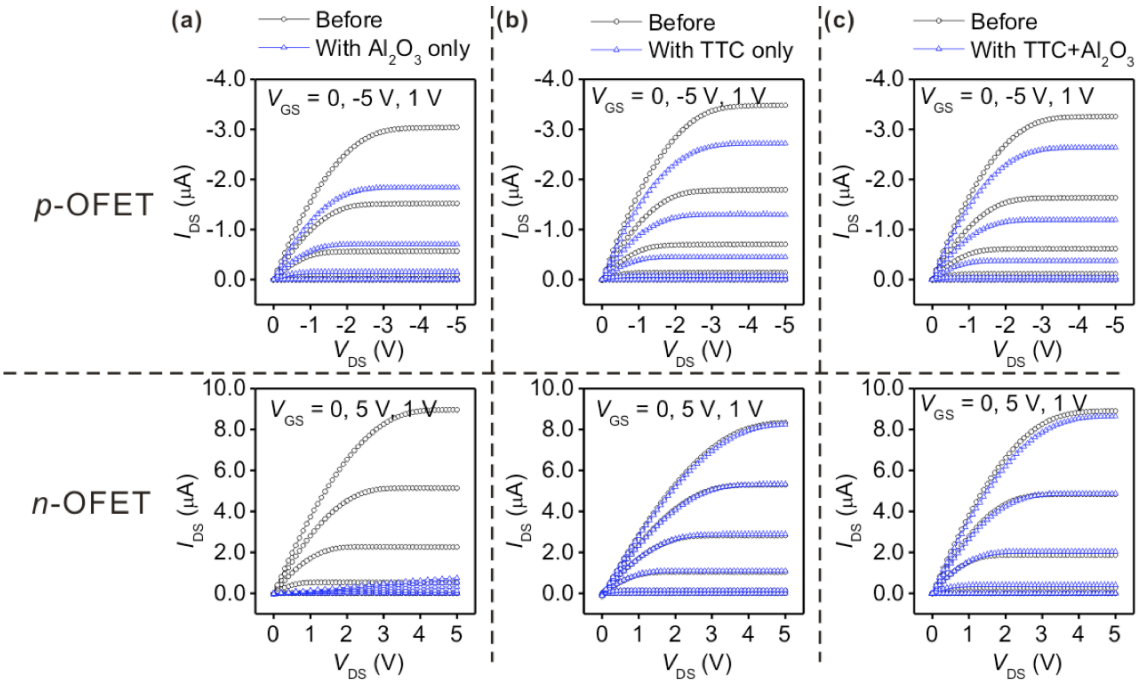


Figure 5.14: Electrical characteristics of *p*-channel and *n*-channel OFETs before encapsulation and after encapsulation with Al_2O_3 only (a), with TTC only (b), and with TTC and Al_2O_3 (c).

Figure 5.14 compares the output electrical characteristics before and after encapsulation for both *p*-channel pentacene and *n*-channel C_{60} OFETs. As described earlier, sample A was coated directly with a layer of Al_2O_3 by ALD without any protective layer. After coating with Al_2O_3, the pentacene *p*-channel OFETs were still functional with the maximum channel current decreasing about 40%, as shown in Figure

5.14(a). However, the *n*-channel C_{60} OFET showed severely inhibited functionality with the channel current decreasing by more than 90%. The current drop was caused by the O_2 and H_2O exposure during the handling, exposure to H_2O vapor (as a precursor) and low vacuum level (10^{-3} torr) during the Al_2O_3 deposition.

Sample B was designed to test if there was any initial damage caused by the deposition of the protective layer (i.e., TTC), so the TTC layer was deposited under high vacuum and the sample was not exposed to O_2 or H_2O at any point (the sample was transferred in a sealed vacuum tube). Even though there was a small current drop of 20% in the *p*-channel OFETs, the TTC layer did not cause any change in the *n*-channel OFETs as shown in Figure 5.14(b). From the study shown in Chapter 3 and Chapter 4, pentacene films exhibited orderly polycrystalline microstructures while C_{60} films were amorphous with an isotropic molecular shape. It can be speculated that the deposition of TTC may have an adverse impact on the crystalline structure in pentacene films that caused the slight device performance degradation in *p*-channel OFETs.

Sample C was designed to test how well the TTC layer can protect the sample from the following encapsulation process. Sample C went through the same deposition process of TTC as sample B, but was followed by the deposition of Al_2O_3 using ALD. Sample C was briefly exposed to air after the coating with TTC and Al_2O_3 during transferring for electrical testing. The change in electrical characteristics was almost identical to the ones with only TTC, as seen in Figure 5.14(c), which demonstrates the effective protection of TTC from the brief O_2 /H_2O exposure and ALD deposition.

The voltage transfer characteristics of inverters before and after encapsulation of sample C were shown in Figure 5.15. With low threshold voltages in both the *p*-channel

and *n*-channel OFETs, the complementary inverters can be operated at a supply voltage V_{DD} as low as 2 V, which is even lower than the values obtained on a plastic substrate in Section 5.2. Even though the device performance of the *p*-channel OFETs slightly degraded from the encapsulation, there was no change in the shape of VTC or decrease in dc gain as shown in Figure 5.15. This can be greatly attributed to the stability of threshold voltage during the encapsulation.

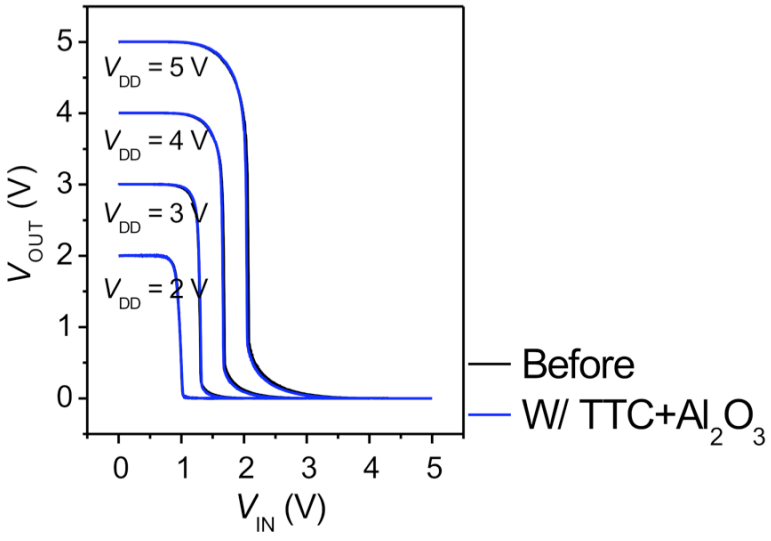


Figure 5.15: Voltage transfer characteristics of inverters before and after encapsulation with TTC and Al_2O_3.

5.3.4 Conclusions

We have demonstrated an effective protection of OFETs and inverters using TTC from O_2/H_2O exposure and from the initial damage caused by the subsequent ALD deposition. Without the protective layer, i.e., TTC, *n*-channel C_{60} OFETs did not function

properly after the deposition of Al_2O_3 by ALD. A TTC layer deposited prior to the deposition of Al_2O_3 can keep the electrical characteristics of C_{60} OFETs intact. The fact that the TTC deposition did not affect the *n*-channel transport can be greatly attributed to the amorphous nature of C_{60} films. Slight device degradation in *p*-channel OFETs was observed with the deposition of TTC or Al_2O_3. The degradation seems inevitable since the polycrystalline film microstructure of pentacene films is susceptible to any deposition/coating process on top of it. However, the degradation was greatly decreased with a protective layer of TTC. Despite the slight device degradation in *p*-channel OFETs, the shape of the VTCs and the dc gain in the inverters remained unchanged from the encapsulation.

CHAPTER 6 CONCLUSIONS AND RECOMMENDATIONS

6.1 Conclusions

In this dissertation, extensive study has been preformed to realize organic complementary inverters through the device engineering of OFETs. A great deal of effort for the device engineering has been given to the control and modification of the interfaces directly in contact with the semiconductor layer, which are between the semiconductor and dielectric and between the semiconductor and source/drain electrodes. As for the gate dielectrics, a high quality, high-κ gate dielectric: Al_2O_3 deposited by ALD was adopted in most experiments to provide high capacitance density and low leakage current. It has been shown that the electrical performance and operational stability of OFETs are correlated closely with the dielectric surface properties and microstructural order of the semiconductor layer, especially in the case of pentacene. On the other hand, the issue with contact resistance is far from serious in n-channel OFETs. With different challenges in the development of *p*-channel and *n*-channel OFETs, the dissertation is categorized into three major parts: *p*-channel OFETs (Chapter 3), *n*-channel OFETs (Chapter 4), and the integration of *p*-channel and *n*-channel OFETs (Chapter 5). The summary and the conclusions are as follows.

Section 3.1 focused on the fabrication of high-performance pentacene OFET devices with Al_2O_3 grown by ALD as the gate dielectric material. These transistors were operated in enhancement mode with a zero turn-on voltage and exhibited a low threshold voltage (< -10 V) as well as a low subthreshold swing (< 1 V/decade) and an on/off current ratio larger than 10^6. High mobility values of 1.5 ± 0.2 cm^2/Vs and 0.9 ± 0.1

cm^2/Vs were obtained when using n^{++}-Si and ITO-coated glass as substrates (also act as gate electrodes), respectively. AFM images of pentacene films on Al_2O_3 revealed well-ordered island formation, and X-ray diffraction patterns showed characteristics of a "thin film" phase. The results of this work not only demonstrate that gate dielectrics grown by ALD present a viable alternative to dielectrics from traditional deposition techniques, but also show that the ALD dielectrics can result in improved electrical performance of transistors even on substrates with high roughness. The latter will become an increasingly critical issue in future for most flexible substrates of interest.

Section 3.2 targeted another remaining problem to be solved in pentacene OFETs: operational instability, including hysteresis, reproducibility and reliability, and bias stress (BS) effect. In this work, the structural ordering, the electrical performance and the operational stability of pentacene OFETs were studied based on PS and BCB polymeric dielectric interfaces and OTS-treated surface dielectrics. Both BCB and PS provided smooth dielectric surfaces with low surface energy, which are attributed to the formation of orderly microstructures of pentacene films with large grain size, and therefore the high electrical performance of pentacene OFETs. However, when measured under prolonged dc gate bias, the electrical performance of devices with BCB deteriorates and the rate is even faster than the devices with OTS-treated dielectric surface. The impurities in the BCB formulation, such as antioxidants, may act as long-lived trapping sites for hole transport. With PS at the gate dielectric surfaces, pentacene OFETs show good electrical performance with low contact resistance as well as extraordinary electrical stability.

Section 4.1 studied the electrical stability of C_{60} *n*-channel OFETs in which the interface between the semiconductor and the gate dielectric was modified with different

polymeric layers and OTS SAM. Studies of electrical degradation under dc bias stress have shown that hydroxyl-free polymers such as BCB, PS, and PMMA can lead to devices with excellent reproducibility and good electrical stability in which interface charge trapping effects are minimized. Our experimental results indicate the electrical instability of C_{60} OFETs with OTS originates from charge trapping at or near the SiO_2 surface, where the surface silanol groups cannot be fully passivated by siloxane-based SAMs [128]. C_{60} OFETs with BCB at the dielectric surface showed the best overall performance with high electron field-effect mobility values that range from 2.7 cm^2/Vs to 5.0 cm^2/Vs, depending on the device geometry, threshold voltages near zero ($|V_T| < 1$ V), low subthreshold slopes (< 0.7 V/decade), and on/off current ratios larger than 10^6.

In Section 4.2, C_{60} OFETs were further improved to have excellent operational stability, high electrical performance as well as low operating voltage and low contact resistance by engineering the essential electrode/semiconductor and dielectric/semiconductor interfaces. By using Ca as the source and drain electrodes, the width-normalized contact resistance (R_cW) at the electrode/semiconductor could be reduced to a constant value of 2 kΩ-cm at a gate-source voltage (V_{GS}) of 2.6 V, leading to electrical properties that are dominated by gate-modulated resistance of the channel as in conventional MOSFETs. Channel length scaling of the source-drain current and transconductance is observed, and average charge mobility values of 2.5 cm^2/Vs extracted at $V_{GS} < 5$ V are found independent of channel length within the studied range. With a low contact resistance, a maximum transconductance g_m larger than 15 μS/mm was achieved, along with excellent electrical stability under multiple test cycles (100 times) and continuous electrical stress were demonstrated. A mobility of 3.2 cm^2/Vs

corrected for contact resistance is shown to be independent of the nature of the metal contact. The combined operating properties of these OFETs, obtained in a N_2-filled glovebox, are comparable to the best *p*-channel OFETs and outperform those of amorphous silicon thin-film transistors.

Proper interface engineering strategies at the dielectric/semiconductor and at the electrode/semiconductor were established in Chapter 3 and Chapter 4 to obtain both *p*-channel and *n*-channel OFETs with high electrical performance, low operation voltage and good operational stability. In order to integrate these OFETs onto the same substrate for inverters, one dielectric surface, which is compatible with both *p*-type and *n*-type semiconductor (pentacene and C_{60} in this work), is necessary to avoid the complicated patterning procedures. Considering the results from both *p*-channel and *n*-channel OFETs, PS was selected to modify the dielectric surface in the fabrication of organic complementary inverters in Chapter 5.

Section 5.2 demonstrated flexible low-voltage organic complementary inverters with both high noise margin and high dc gain using pentacene and C_{60} as active semiconductors fabricated on a plastic substrate. With the surface of gate dielectrics passivated with a thin layer of PS, both *n*-channel and *p*-channel OFETs show negligible hysteresis and comparable threshold voltages. The inverters can be operated at a supply voltage as low as 3 V with noise margin values higher than 80% of their maximum theoretical value. A high dc gain of 180 was obtained at a supply voltage of 5 V. The inverters demonstrated good mechanical stability when tested after bending under both tensile and compressive stress.

Section 5.3 discussed an issue regarding the air stability of OFETs and inverters and preliminary research on the encapsulation with a protective layer was performed. With an additive layer of TTC, the underlying OFETs and inverters were effectively protected from the O_2/H_2O exposure and from the initial damage caused by the subsequent ALD deposition. Without the protective layer, i.e., TTC, *n*-channel C_{60} OFETs was not able to function properly even with brief exposure to the air. The deposition of a TTC layer did not disturb the electrical characteristics of C_{60} OFETs, probably benefiting from the amorphous nature of C_{60} films. Slight device degradation in *p*-channel OFETs was observed with the deposition of TTC or Al_2O_3. The degradation seems inevitable since the polycrystalline film microstructure of pentacene films is susceptible to any deposition/coating process on top of it. However, the degradation was greatly decreased with a protective layer of TTC. Despite the slight device degradation in *p*-channel OFETs, the shape of VTC and the dc gain in the inverters remained unchanged from the encapsulation.

6.2 Recommendations for Future Work

The first recommendation for the future work is to further improve the electrical performance for *p*-channel pentacene OFETs. As we discussed in Chapter 1, in order to take full advantage of CMOS technology, it requires that both *p*-channel and *n*-channel OFETs have comparable figures of parameters, such as mobility and threshold voltage. Although C_{60} is a good electron transporter and we achieved low-voltage complementary inverters with high gain and high noise margins, the limitation for the inverter comes from the material with the lower mobility: pentacene. The correlation between the

morphology of pentacene film (i.e., molecule orientation and packing, grain size and boundary) and the charge transport, and device performance has been fully recognized. A direct strategy can be implemented to control the morphology of pentacene film, especially at the first monolayer close the dielectric interface, by tuning the substrate temperature, deposition rate and film thickness during the pentacene deposition. Since higher purity correlates with higher performance, sublimation of pentacene starting materials multiple times is preferred. In addition, the deposition rate of the top source/drain electrodes is another factor to consider. The deposition of electrodes could lead to the diffusion of metal molecules into the pentacene films and have a direct impact on the morphology.

The lifetime of the OFETs and inverters in air can be prolonged by proper encapsulation. To do so, two or more alternative depositions of oxide and polymer layers are required. Since we have identified TTC as a good protective layer, the preferred structure for the encapsulation could be TTC/Al_2O_3/Parylene/Al_2O_3/Parylene. External contacts will be needed to avoid the diffusion of O_2/H_2O through the pinholes caused during the testing. Additional edge sealing is probably needed. In the case of C_{60} OFETs, thinner Ca layers can be capped with other stable metals as source/drain contacts to lower the probability of Ca oxidation while maintaining a quasi-ohmic contact with C_{60}. The water permeation rate through the encapsulation layers can be roughly measured using a Ca test, if possible, under standard accelerated testing conditions of 60°C/90% relative humidity (RH). The lifetime testing will be performed outside the N_2-filled glovebox either under ambient conditions or under a controlled RH.

Future work should address several issues with the gate dielectrics. First, gate dielectrics with higher dielectric constant can be used in low power applications. HfO_2 with a dielectric constant of 25, also available in ALD system, holds promise. Secondly, gate insulators should be patterned with minimized overlapping capacitance to increase operating frequency. More consideration can be placed in choosing proper gate electrodes, which is closely related to the charge injection/extraction, Fermi-level shift, etc.

As for flexible devices, the usage of inorganic oxides as gate dielectrics could eventually lead to cracks and structural defects in the film under mechanical stress. The strain on the oxide can be alleviated by placing it in a neutral position sandwiched between two layers of polymers. Mechanical modeling and calculation will be needed to determine the thickness of each layer.

6.3 A List of Selected Publications

1. **Xiao-Hong Zhang** and Bernard Kippelen, "Low-voltage flexible organic complementary inverters with high noise margin and high dc gain", Applied Physics Letters **94**, 043312, 2009.
2. **Xiao-Hong Zhang** and Bernard Kippelen, "High-performance *n*-channel C_{60} organic field-effect transistors through interface optimization", Journal of Applied Physics **104**(10), 104504, 2008.
3. **X.-H. Zhang** and B. Kippelen, "Low voltage C_{60} organic field-effect transistors with high mobility and low contact resistance", Applied Physics Letters **93**, 1, 2008.
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